Model Name : A5WAM
File Name : LA-B981P

Compal Confidential

EA51_BM DIS M/B Schematics Document

Intel Bay Trail M + N15V-GL/N15V-GM

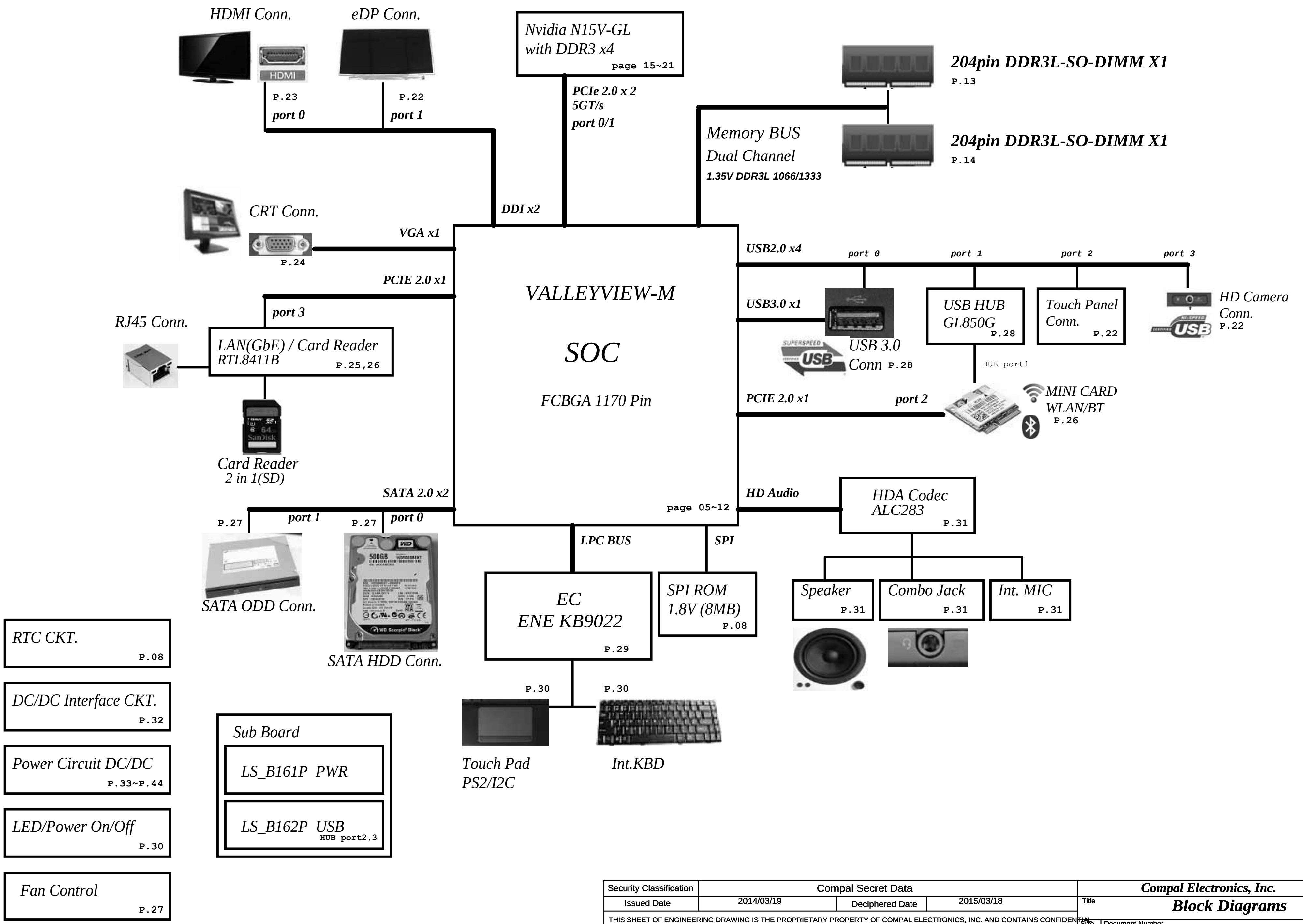
2014-05-12

REV:0.1

PCB@
DAX PCB 15Y LA-B981P REV0 MB 2

Part Number	Description
DA60019D000	PCB 15Y LA-B981P REV0 MB 2

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Issued Date	2014/03/19	Deciphered Date	2015/03/18	Title: Cover Page
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Size: Custom | Document Number: A5WAM_Bay Trail M_LA-B981P | Rev 0.1

Voltage Rails

Power Plane	Description	S0	S3	S4/S5
VIN	19V Adapter power supply	ON	ON	ON
BATT+	12V Battery power supply	ON	ON	ON
B+	AC or battery power rail for power circuit. (19V/12V)	ON	ON	ON
+RTCVCC	RTC Battery Power	ON	ON	ON
+1.0VALW	+1.0v Always power rail	ON	ON	ON
+1.8VALW	+1.8v Always power rail	ON	ON	ON
+3VALW	+3.3v Always power rail	ON	ON	ON
+5VALW	+5.0v Always power rail	ON	ON	ON
+1.35V	+1.35V power rail for DDR3L	ON	ON	OFF
+3V_PTP	+3.3V power rail for PTP	ON	ON	OFF
+SOC_VCC	Core voltage for SOC	ON	OFF	OFF
+SOC_VNN	GFX voltage for SOC	ON	OFF	OFF
+0.675VS	+0.675V power rail for DDR3L Terminator	ON	OFF	OFF
+1.0VS	+1.0v system power rail	ON	OFF	OFF
+1.05VS	+1.05v system power rail	ON	OFF	OFF
+1.35VS	+1.35v system power rail	ON	OFF	OFF
+1.5VS	+1.5v system power rail	ON	OFF	OFF
+1.8VS	+1.8v system power rail	ON	OFF	OFF
+3VS	+3.3v system power rail	ON	OFF	OFF
+5VS	+5.0v system power rail	ON	OFF	OFF
+3VSDGPU	+3.3V dGPU power rail	ON**	OFF	OFF
+VGA_CORE	Core voltage for dGPU	ON**	OFF	OFF
+1.5VSDGPU	+1.5V dGPU power rail	ON**	OFF	OFF
+1.05VSDGPU	+1.05V dGPU power rail	ON**	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

Note : ON** dGPU optimus on

Board ID / SKU ID Table for AD channel

Vcc	3.3V
Ra	100K +/- 1%

Board ID	Rb	V min	V typ	V max	EC AD
0	0		0.000V	0.300V	0x00 - 0x0B
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C - 0x46
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA3
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA4 - 0xAD
13	240K +/- 1%	2.316V	2.329V	2.343V	0xAE - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xC0
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC1 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD3
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD4 - 0xDC
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDD - 0xE6
19	NC	3.000V	3.300V		0xE7 - 0xFF

BOARD ID Table_LA-B212

Board ID	PCB Revision
10	EVT_LA-B212PR01
11	PVT_LA-B981PR01

43 level BOM table

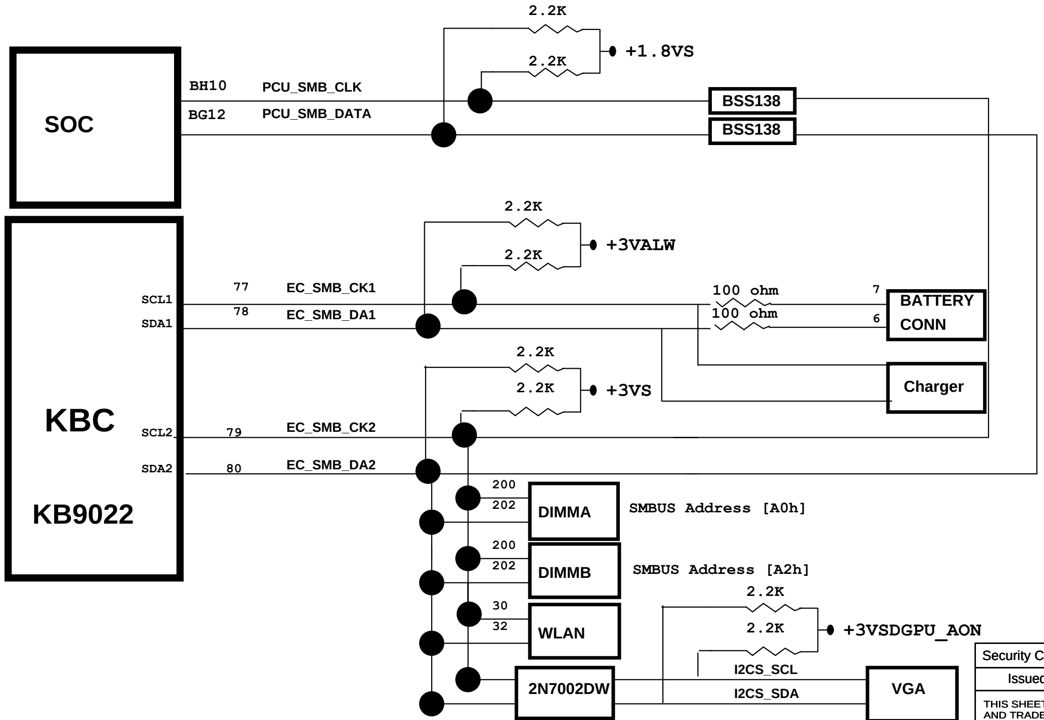
43 Level	Description	BOM Structure
4319URBOL01	SMT MB AB212 A5WAM GM2G N3530 HDMI	N3530@/9022@/DBG@/EMC@/PCB@/1DMIC@/NTPM@/VGA@/VGM@/X762G@
4319URBOL02	SMT MB AB212 A5WAM GL1G N2930 HDMI	N2930@/9022@/DBG@/EMC@/PCB@/1DMIC@/NTPM@/VGA@/VGL@/X761G@
4319URBOL03	SMT MB AB212 A5WAM GL1G N2830 HDMI	N2830@/9022@/DBG@/EMC@/PCB@/1DMIC@/NTPM@/VGA@/VGL@/X761G@
4319URBOL04	SMT MB AB212 A5WAM GL1G N3530 HDMI	N3530@/9022@/DBG@/EMC@/PCB@/1DMIC@/NTPM@/VGA@/VGM@/X761G@
4319URBOL05	SMT MB AB212 A5WAM GM2G N2930 HDMI	N2930@/9022@/DBG@/EMC@/PCB@/1DMIC@/NTPM@/VGA@/VGL@/X762G@
4319URBOL06	SMT MB AB212 A5WAM GM2G N2830 HDMI	N2830@/9022@/DBG@/EMC@/PCB@/1DMIC@/NTPM@/VGA@/VGL@/X762G@

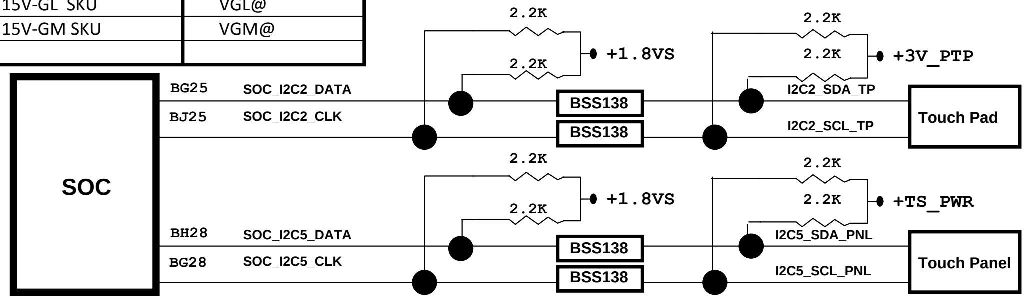
BOM Option Table

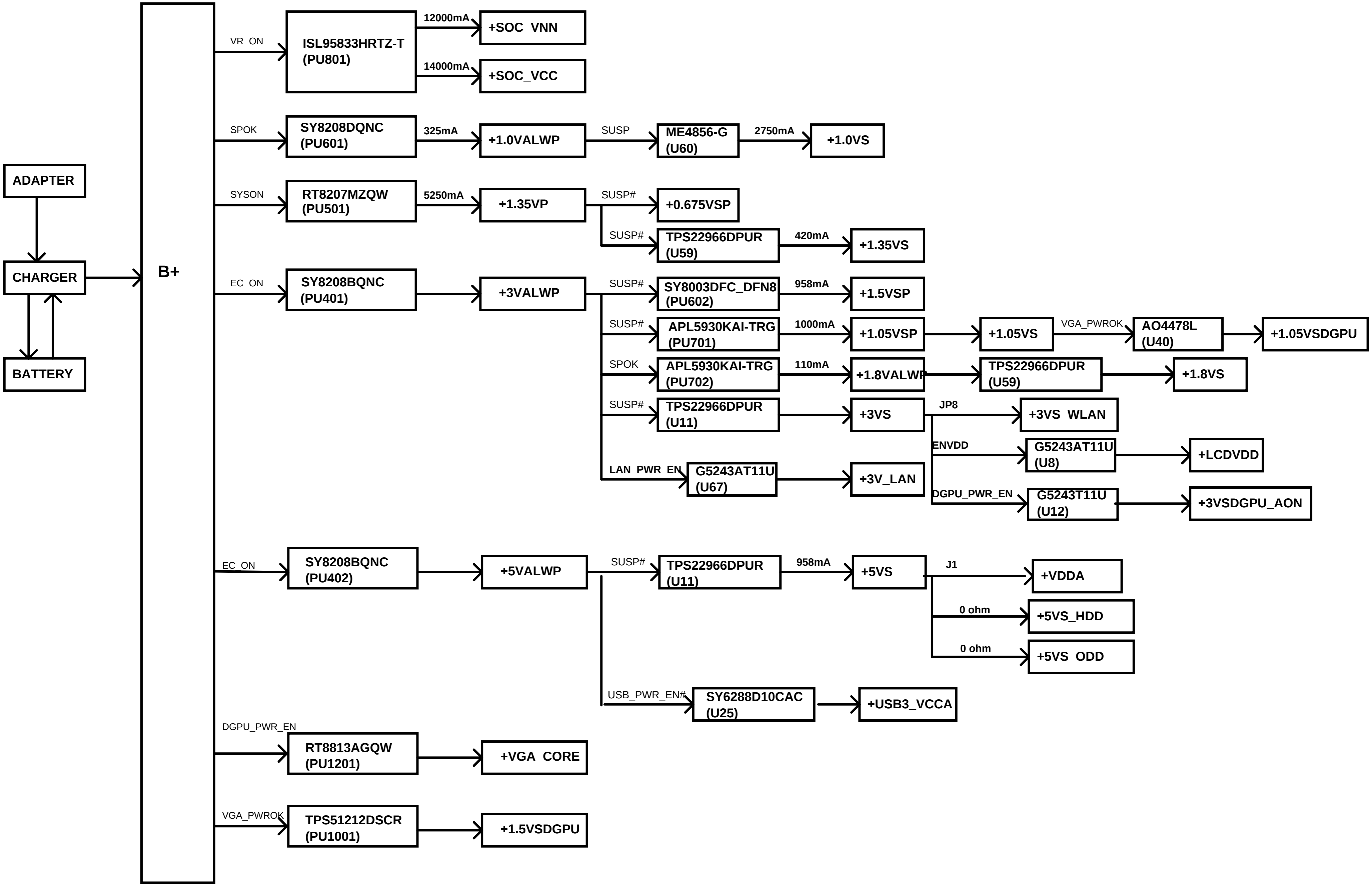
Item	BOM Structure
Unpop	@
Connector	CONN@
EMC requirement	EMC@
EMC requirement depop	@EMC@
KB9012	9012@
KB9022	9022@
Touch Screen I2C	TSI@
KB BL	BL@
DMIC*1	1DMIC@
DMIC*2	2DMIC@
TPM	TPM@
NTPM	NTPM@
Debug SW	DBG@
dGPU	VGA@
N15V-GL SKU	VGL@
N15V-GM SKU	VGM@

BOM Option Table

Item	BOM Structure
X76 1G VRAM	X761G@
X76 2G VRAM	X762G@
	1GHYN@
	1GFFR@
	1GSAM@
	2GAFR@
	2GSAM@
	2GMIC@







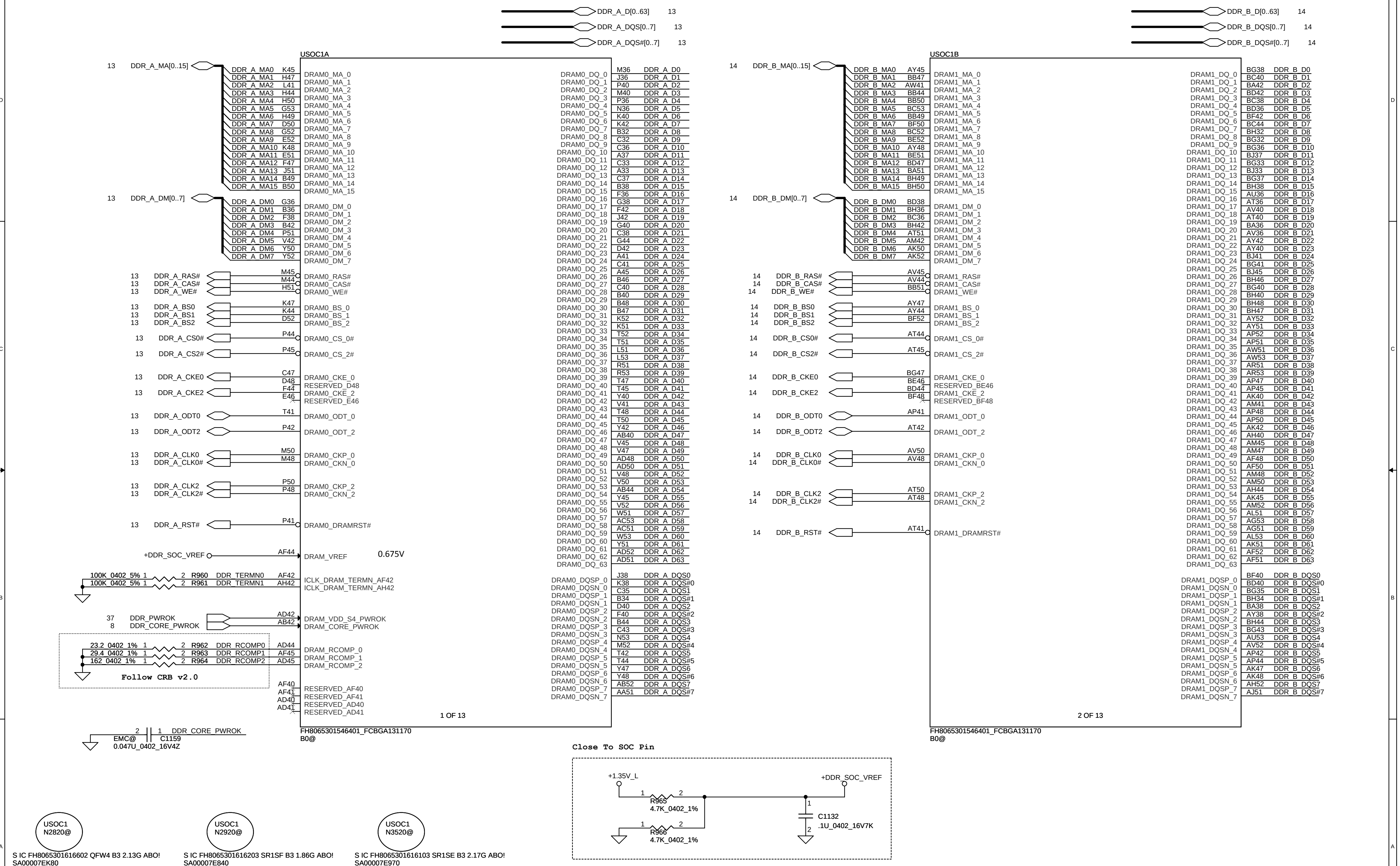
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Title: *Power Rail*

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Date: Monday, May 12, 2014 |



USOC1 N2820@
S IC FH8065301616602 QFW4 B3 2.13G ABO!
SA00007EK80

USOC1 N2920@
S IC FH8065301616203 SR1SF B3 1.86G ABO!
SA00007E840

USOC1 N3520@
S IC FH8065301616103 SR1SE B3 2.17G ABO!
SA00007E970

USOC1 N2830@
S IC FH8065301729602 SR1W4 C0 2.16G ABO!
SA00007QRD0

USOC1 N2930@
S IC FH8065301729501 SR1W3 C0 1.83G ABO!
SA00007RVB0

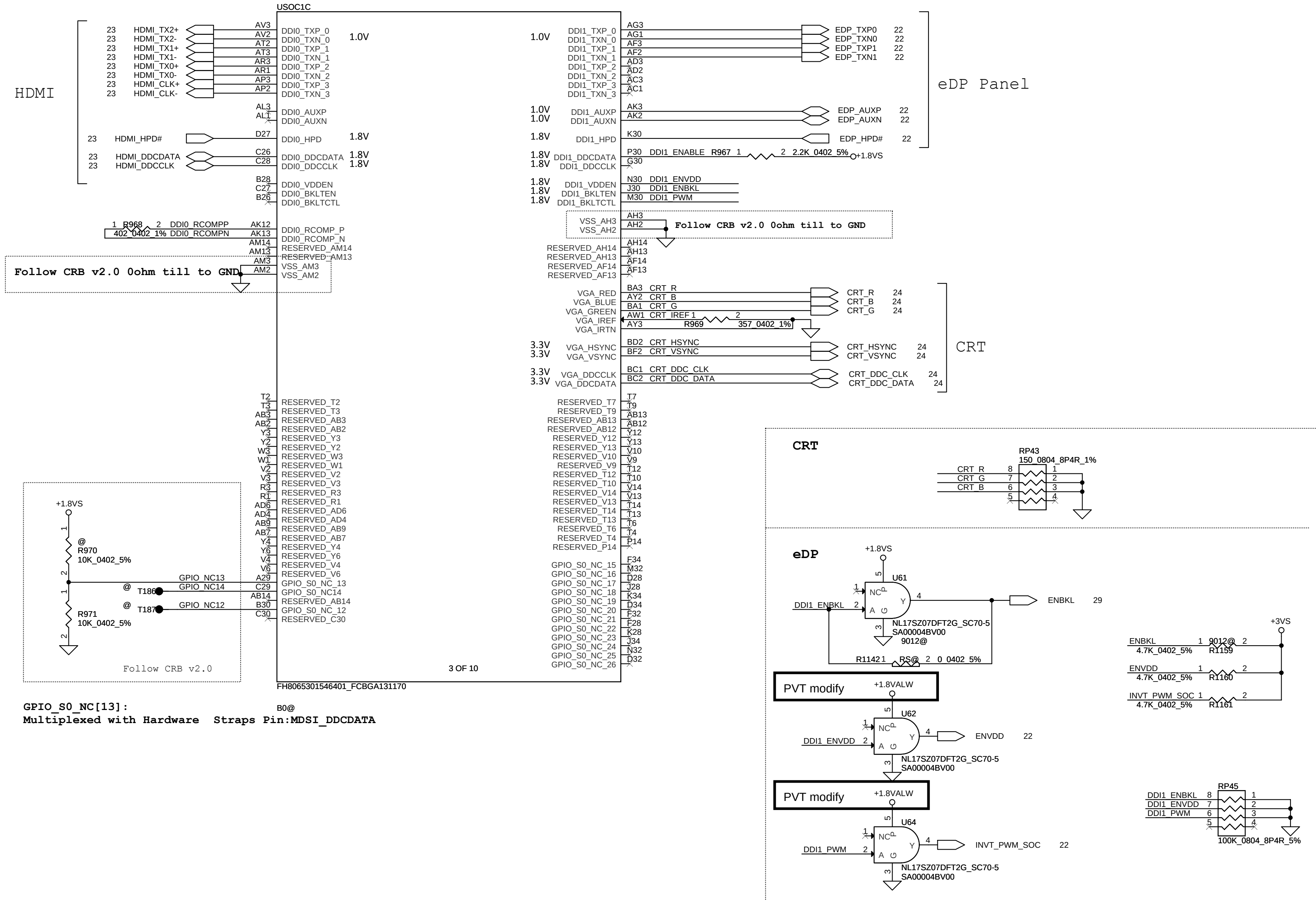
USOC1 N3530@
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Issued Date	2014/03/19	Deciphered Date	2015/03/18

Compal Electronics, Inc.

Title: **VLV-M SOC Memory DDR3L**

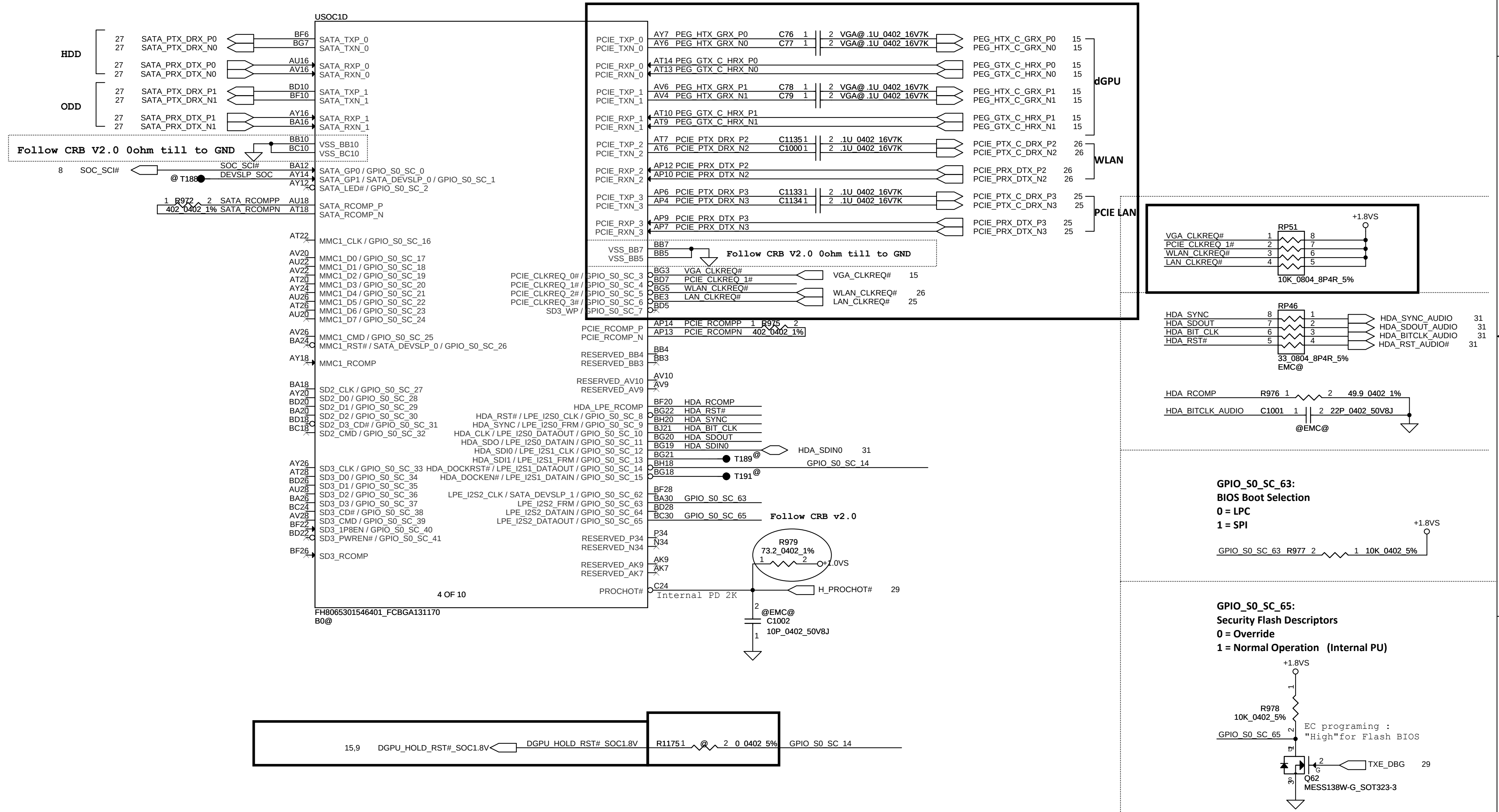
Size: Custom | Document Number: **A5WAM_Bay Trail M_LA-B981P** | Rev: 0.1



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Issued Date	2014/03/19	Deciphered Date	2015/03/18	Title: VLV-M SOC Display
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				Date: Monday, May 12, 2014; Sheet 6 of 47

Follow ACER 2014 X86 HSIO DG V1.03

BAY Trail M		Acer 2014	
USB3 Port1		USB 3 (I/O)	
PCIe Port0		dGPU/M.2 PCIE	LAN
PCIe Port1			WIFI
PCIe Port2		WIFI	
PCIe Port3		LAN+CR	



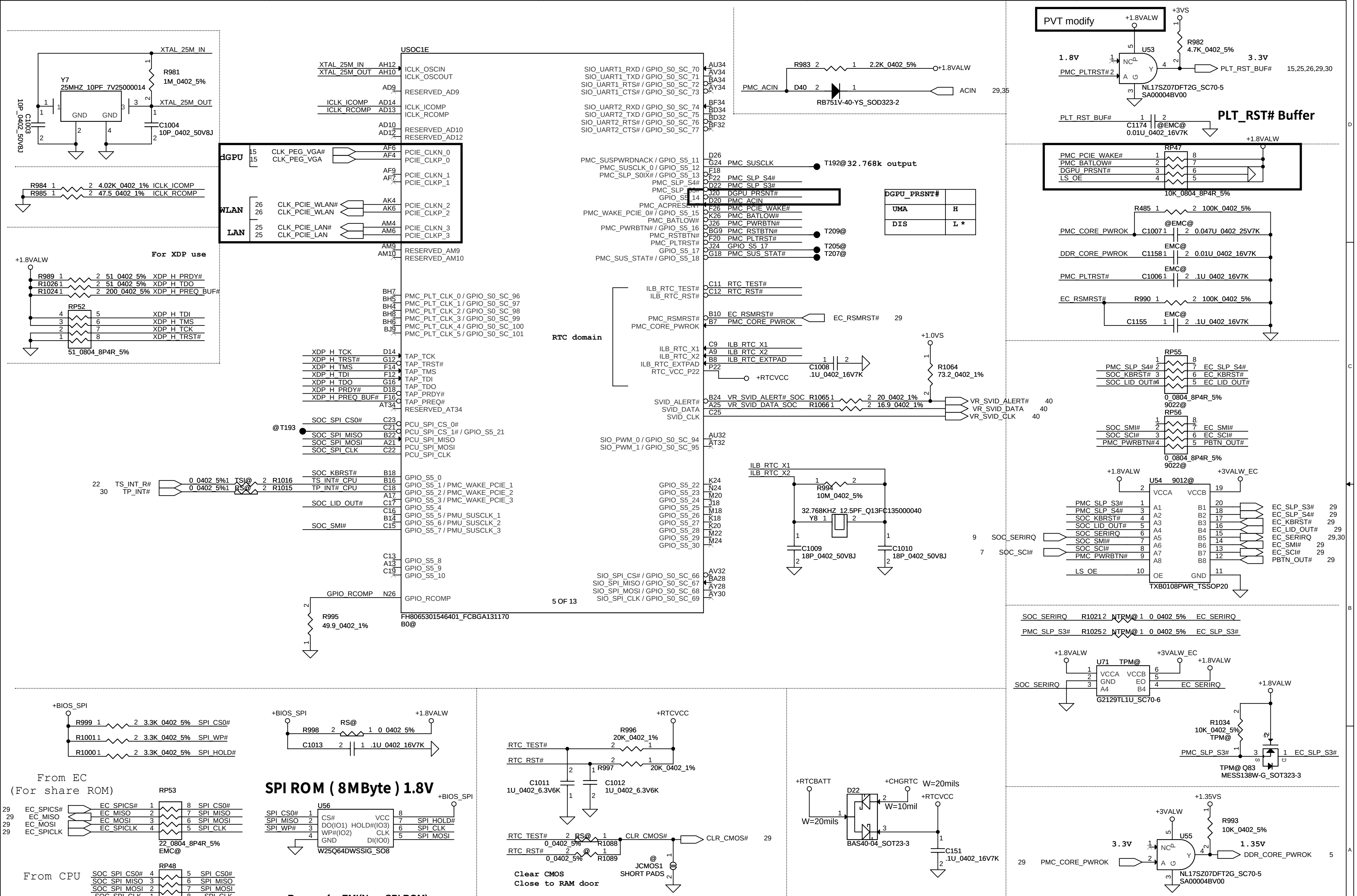
Security Classification	Compal Secret Data		
Issued Date	2014/03/19	Deciphered Date	2015/03/18

Compal Electronics, Inc.

Title: **VLV-M SOC SATA/PCI-E/HDA**

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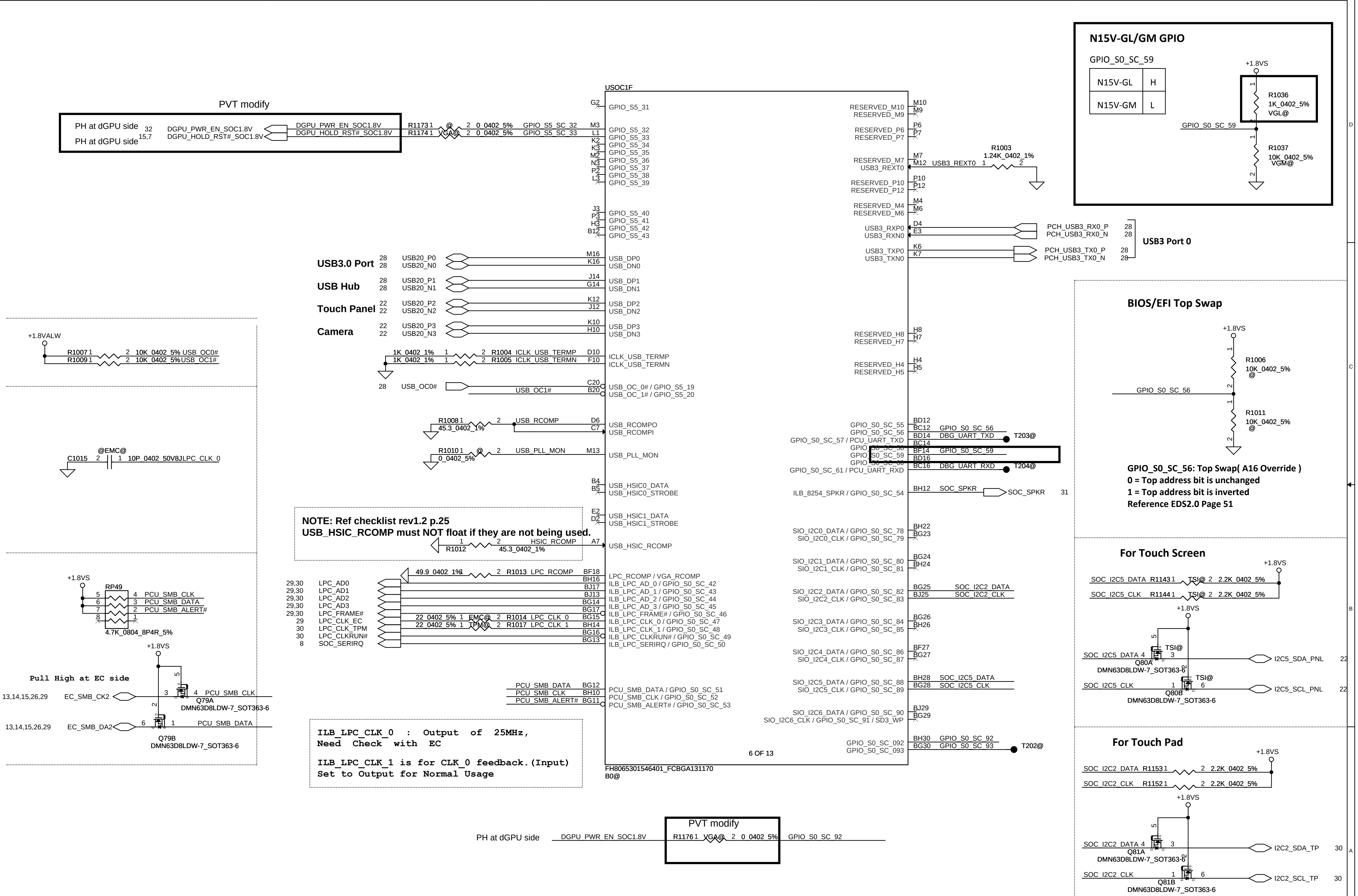
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Compal Electronics, Inc.

Title: *VLV-M SOC CLK/PMU/SPI*

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Date: Monday, May 12, 2014 — Sheet 8 of 47

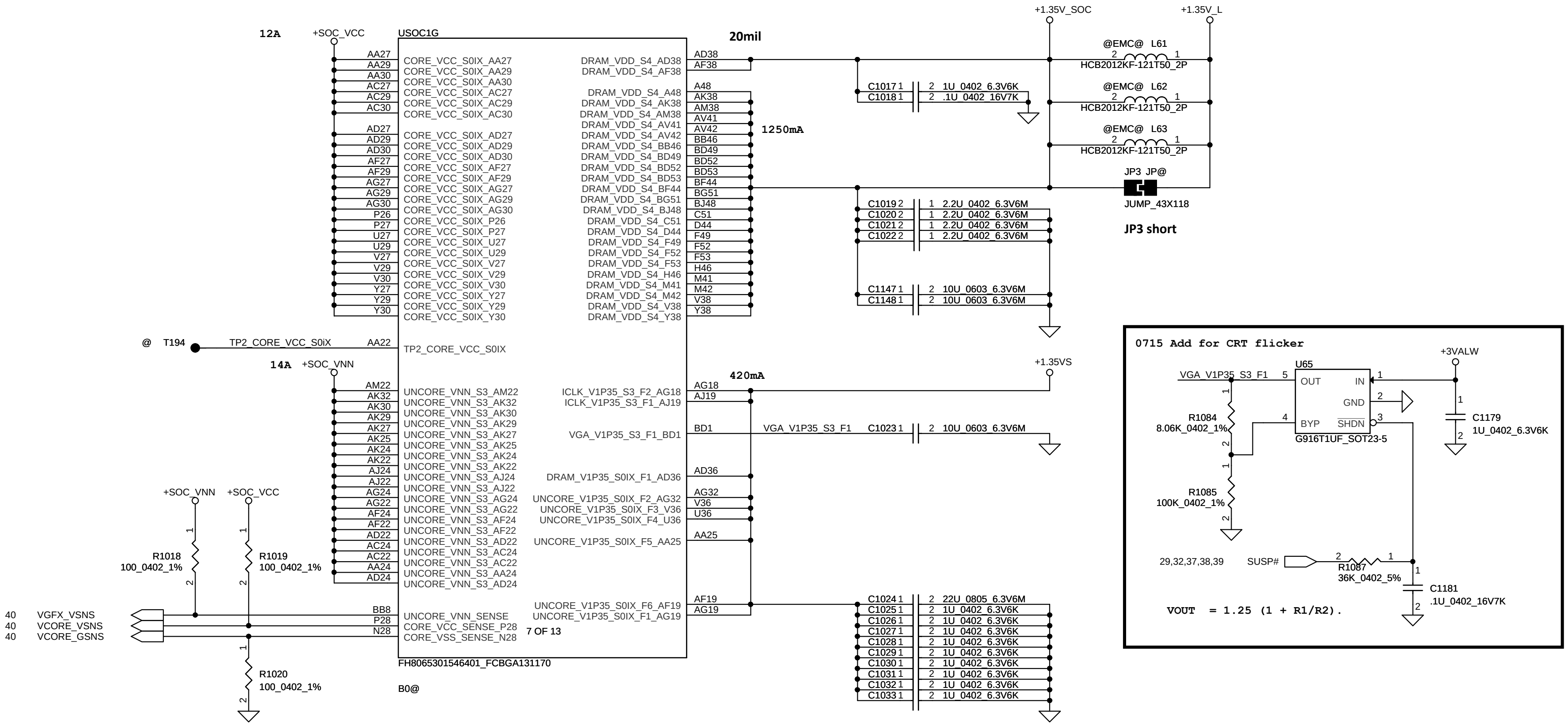


Security Classification	Compal Secret Data		
Issued Date	2014/03/19	Deciphered Date	2015/03/18

Compal Electronics, Inc.

Title: **VLV-M SOC USB/LPC/SMBus**

Size: Custom — Document Number: **A5WAM_Bay Trail M_LA-B981P** — Rev 0.1



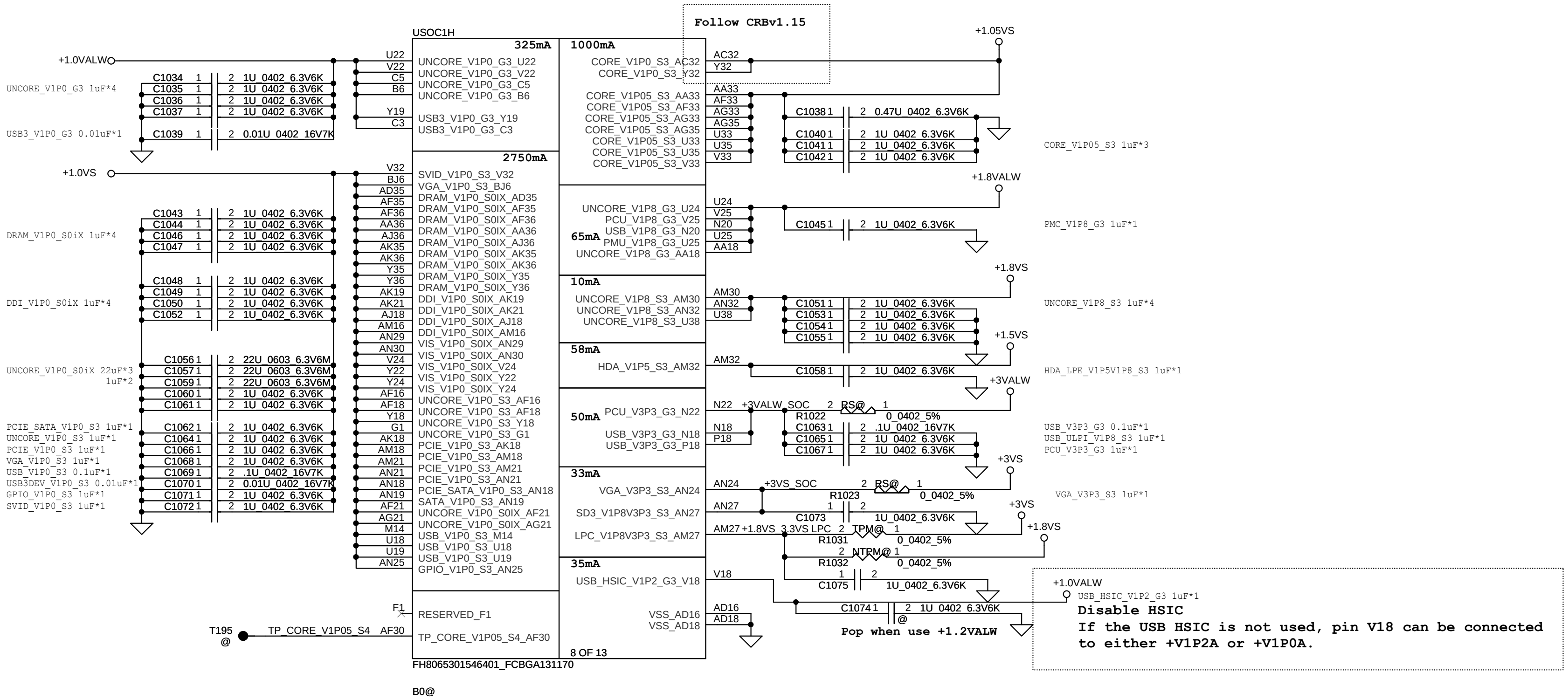
Security Classification	Compal Secret Data		
Issued Date	2014/03/19	Deciphered Date	2015/03/18

Compal Electronics, Inc.

Title: **VLV-M SOC Power**

Size: Custom | Document Number: **A5WAM_Bay Trail M_LA-B981P** | Rev 0.1

Date: Monday, May 12, 2014 |



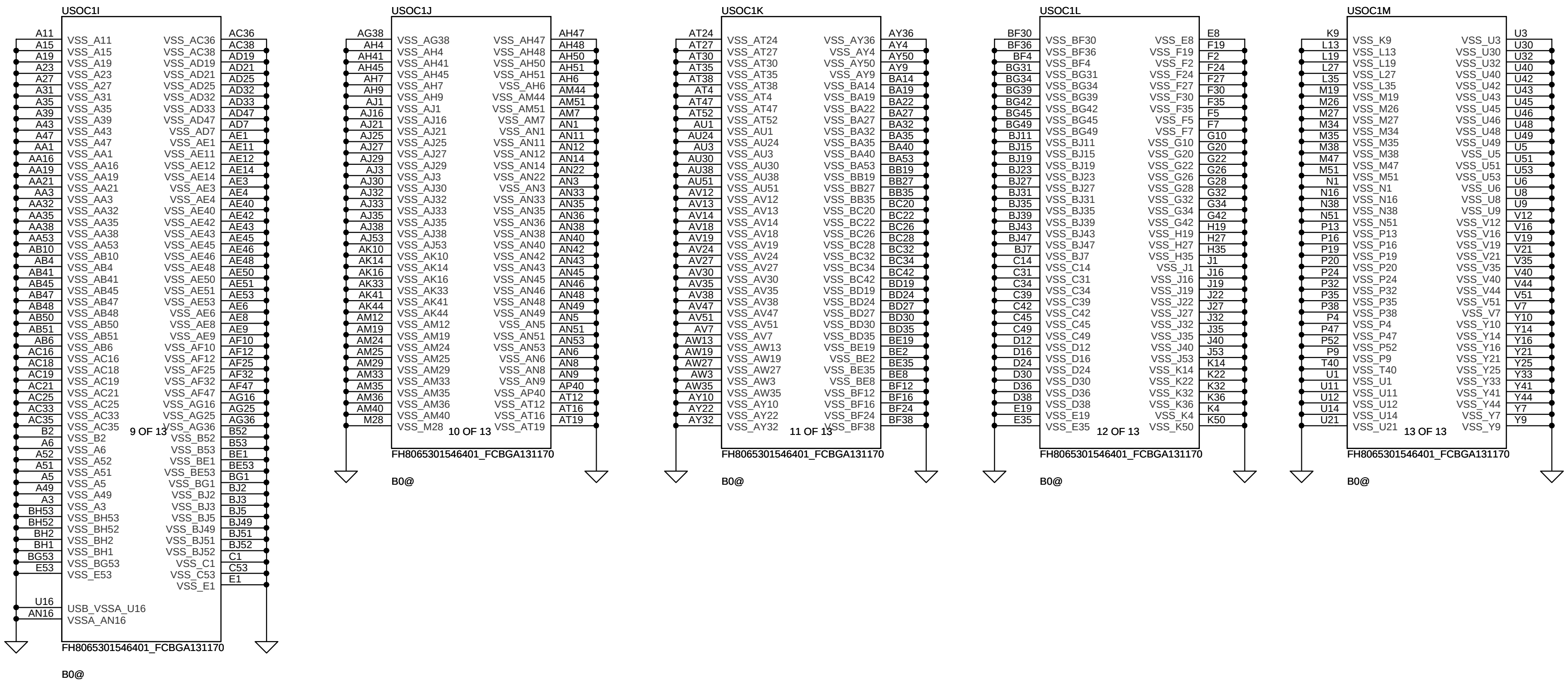
Security Classification	Compal Secret Data		
Issued Date	2014/03/19	Deciphered Date	2015/03/18

Compal Electronics, Inc.

Title: *VLV-M SOC Power*

Size	Document Number	Rev
Custom	A5WAM_Bay Trail M_LA-B981P	0.1

Date: Monday, May 12, 2014 | Sheet 11 of 47



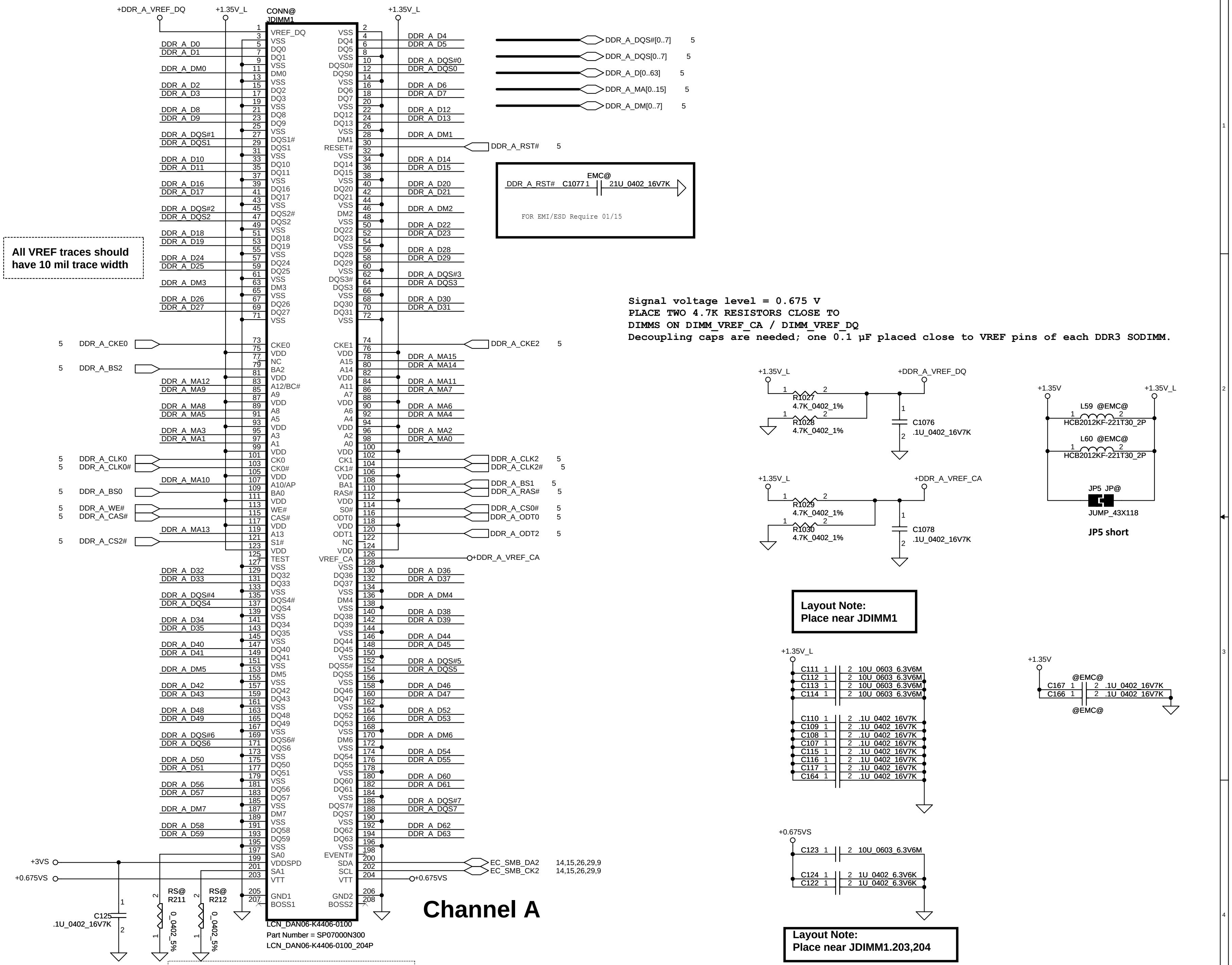
Security Classification	Compal Secret Data		
Issued Date	2014/03/19	Deciphered Date	2015/03/18

Compal Electronics, Inc.

Title: **VLV-M SOC GND**

Size: Custom | Document Number: **A5WAM_Bay Trail M_LA-B981P** | Rev: 0.1

Date: Monday, May 12, 2014 |



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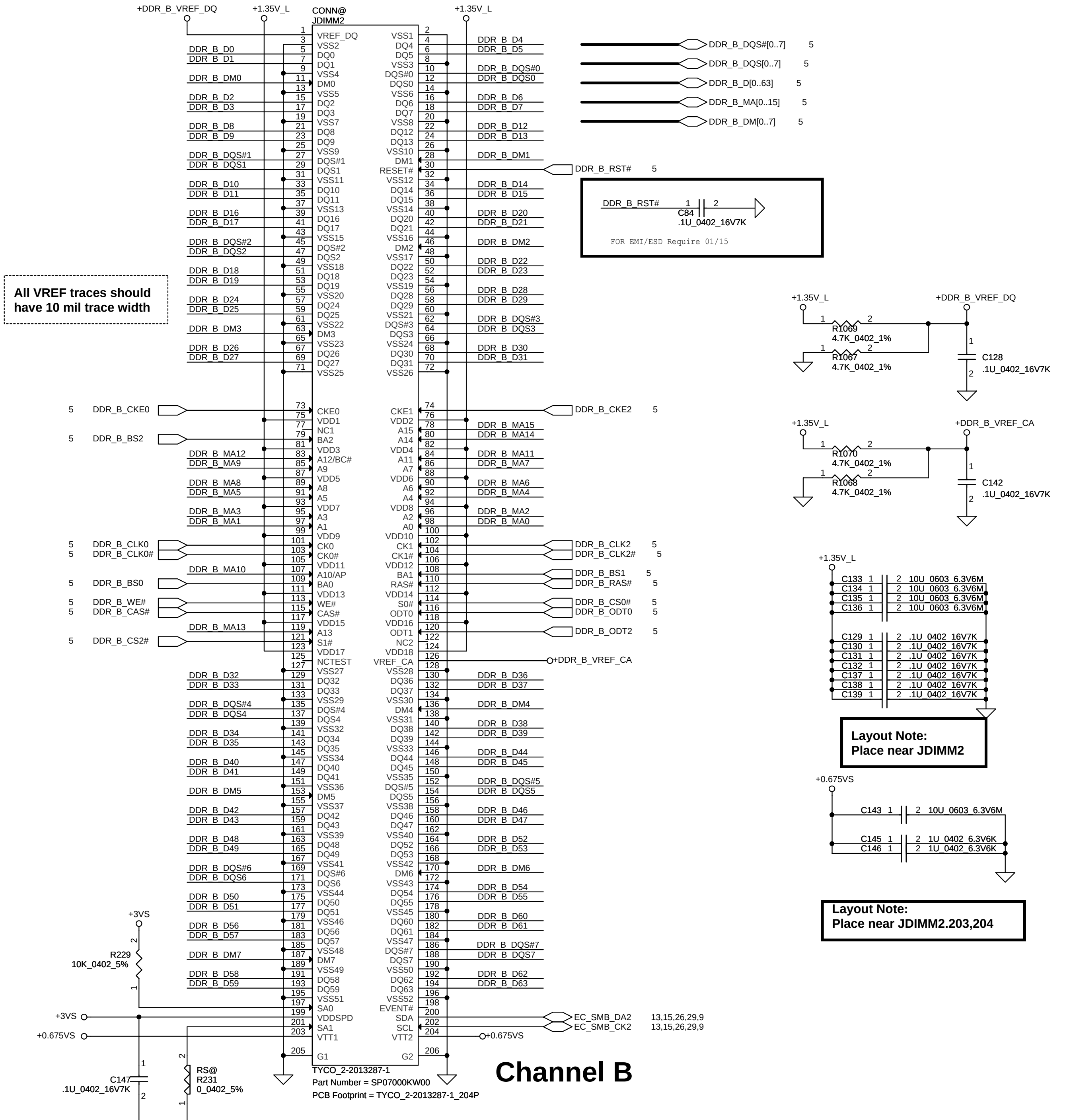
DIMM_1 STD H:4mm

Security Classification	Compal Secret Data		
Issued Date	2014/03/19	Deciphered Date	2015/03/18

Compal Electronics, Inc.

Title: **DDR3L DIMMA**

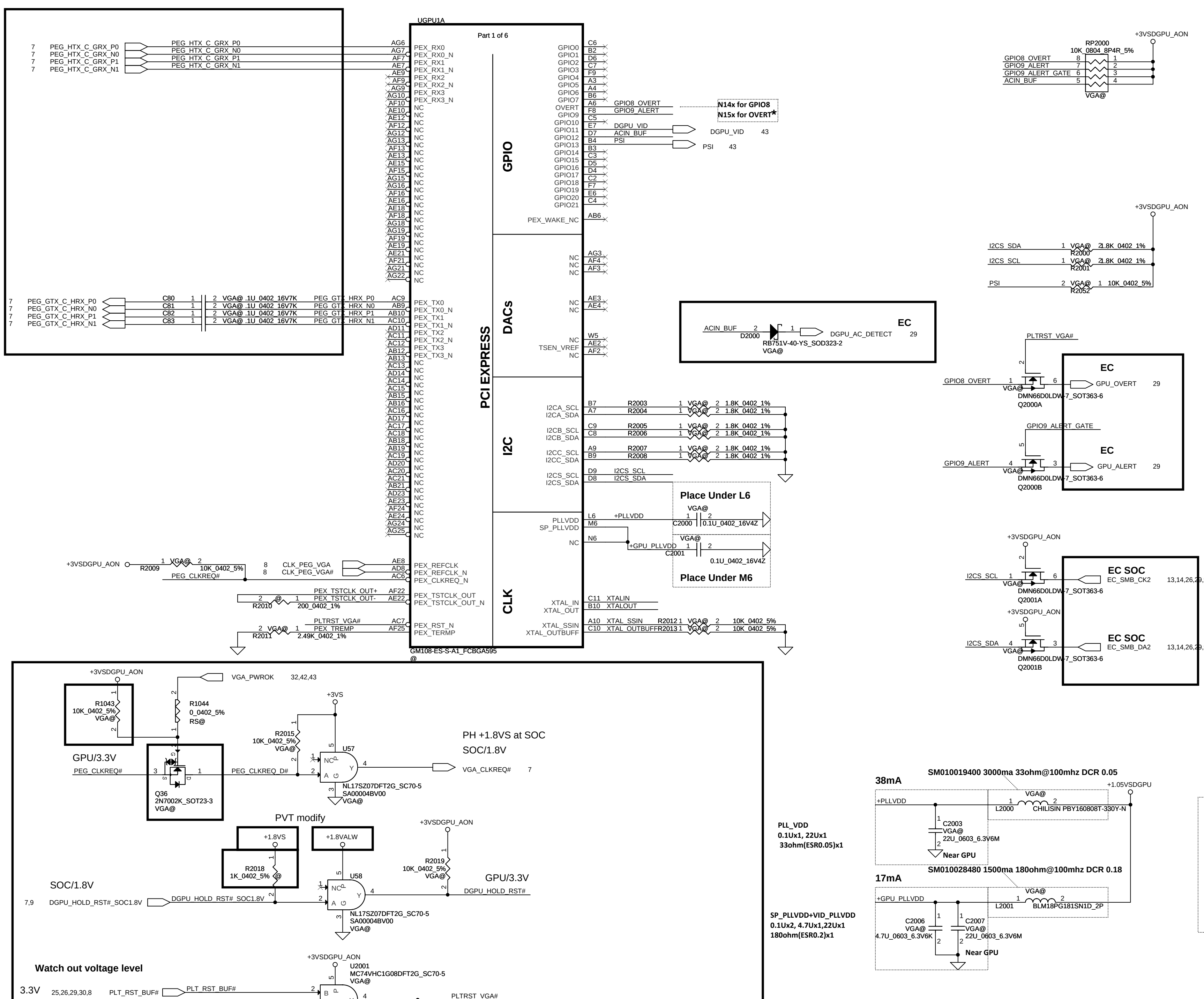
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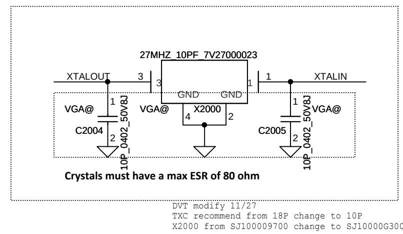


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DIMM_2 REV H:4mm

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GPIO	I/O	USAGE
GPIO0	I	GC6_FB_EN
GPIO1	O	MEM_VDD_CTL
GPIO2	O	LCD_BL_PWM
GPIO3	O	LCD_VCC
GPIO4	O	LCD_BL_EN
GPIO5	O	3V3_MAIN_EN
GPIO6	I	GPU_EVENT#
GPIO7	O	3D Vision
GPIO8	I	SYS_PEX_RST_MON#
GPIO9	I/O	ALERT
GPIO10	O	MEM_VREF_CTL
GPIO11	O	PWM_VID
GPIO12	I	PWR_LEVEL
GPIO13	O	PSI
GPIO14	I	HPD_A
GPIO15	I	HPD_C
GPIO16		RESERVED
GPIO17	I	HPD_D
GPIO18	I	HPD_E
GPIO19	I	HPD_F or HPD_B
GPIO20		Reserved
GPIO21	O	GPU_PEX_RST_HOLD#
GPIO22		
GPIO23		
GPIO24		

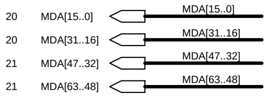
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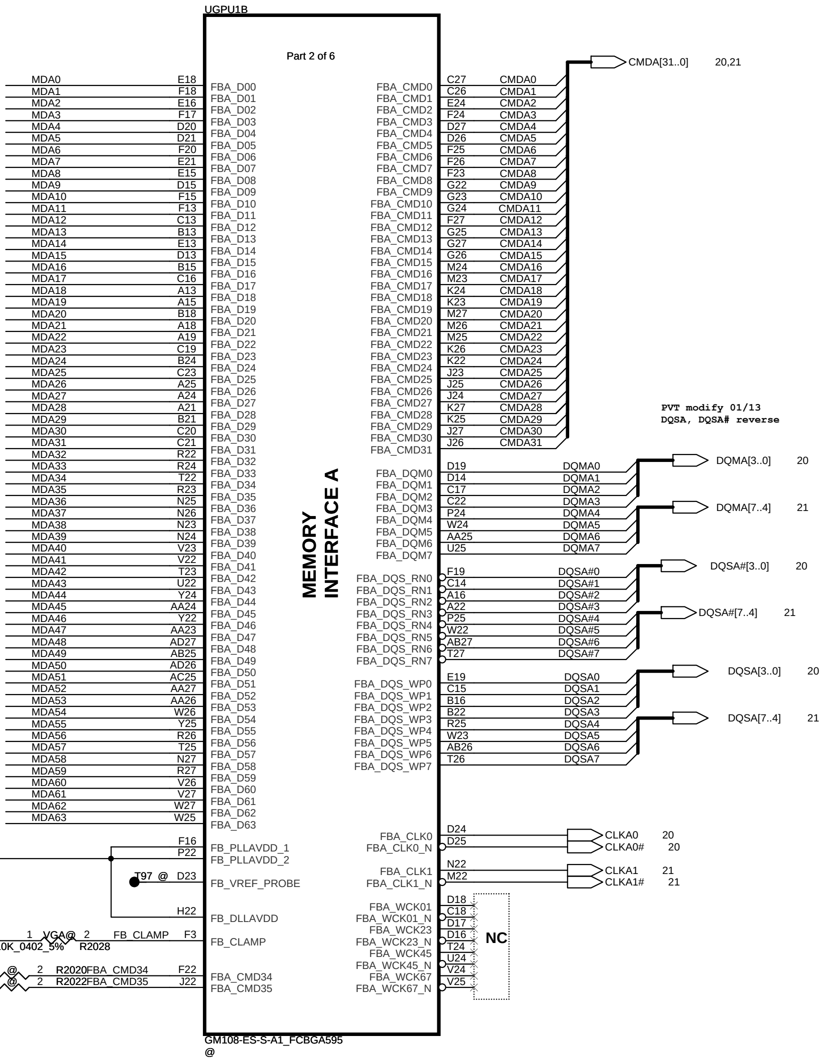
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Title: **N15X PEG 1/7**

Size: Custom | Document Number: **A5WAM_Bay Trail M_LA-B981P** | Rev 0.1

VRAM Interface

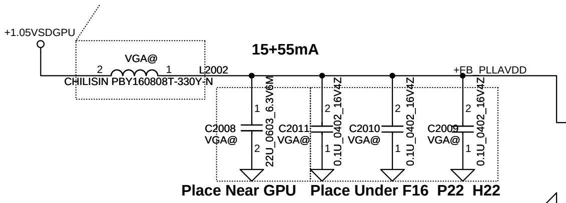




NV 15x DG-06803-V03

GPU Package	Rail	Capacitor Type		Footprint	Population	Location
GB2B-64	FBx_PLL_AVDD and FB_DLL_AVDD Combined	0.1 µF	X7R	0402	2	Under GPU
		22 µF	X5R	0805	1	Near GPU
		Bead Type				
		30 Ω (ESR=0.010 Ω)		0603	1	Near GPU

SM010019400 3000ma 33ohm@100mhz DCR 0.05

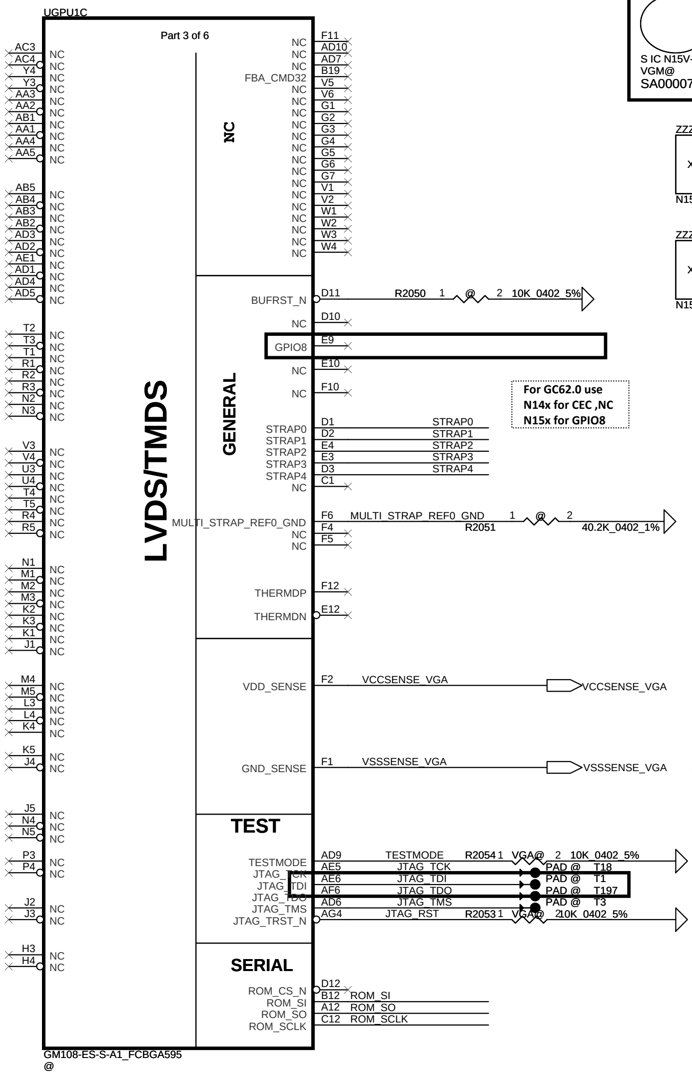


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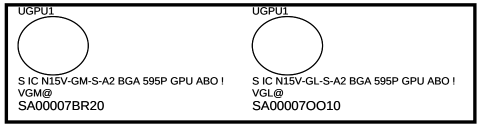
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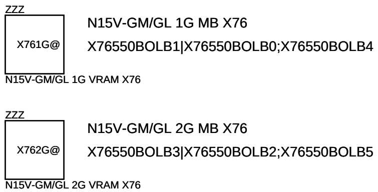
Title: **N15X VRAM 2/7**

Size: Custom | Document Number: **A5WAM_Bay Trail M_LA-B981P** | Rev: 0.1

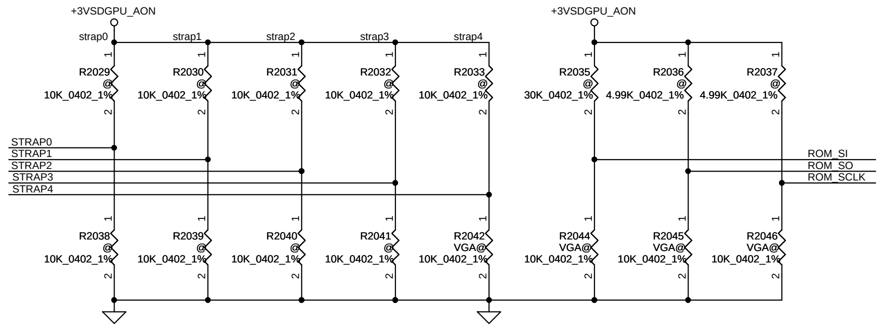


For GC62.0 use
N14x for CEC ,NC
N15x for GPIO8





BINARY LEVEL STRAPS



For N15V-GL/GM Binary strap table

Decive ID : 0x1140

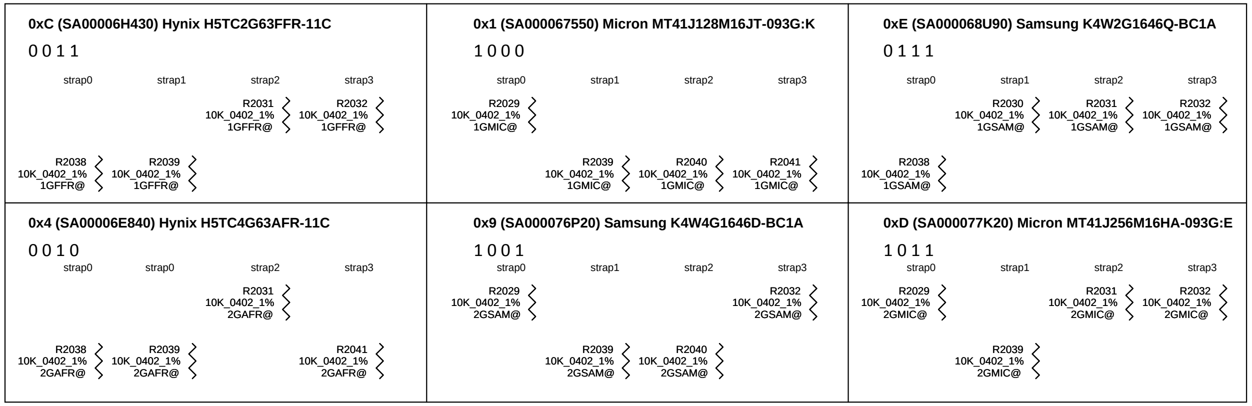
GPU	FBVDD/FBVDDQ	X76	Freq	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N15V-GL N15V-GM	Set +1.5VSDGPU power rail as +1.35V PR1007 9.31K ohm	X76550BOLB0	900MHz	128Mx16x4	0x1 (SA000067550) Micron MT41J128M16JT-093G:K	PU 10K	PD10K	PD 10K	PD 10K	PD 10K	PD 10K	PD 10K	PD 10K
					0x5 (SA000068U00) Samsung K4W2G1646E-BC1A	PU 10K	PD10K	PU 10K	PD 10K				
		X76550BOLB1			0xC (SA00006H430) Hynix H5TC2G63FFR-11C	PD 10K	PD10K	PU 10K	PU 10K				
		X76550BOLB4			0xE (SA000068U90) Samsung K4W2G1646Q-BC1A	PD 10K	PU 10K	PU 10K	PU 10K				
		X76550BOLB5	900MHz	256Mx16x4	0x9 (SA000076P20) Samsung K4W4G1646D-BC1A	PU 10K	PD10K	PD 10K	PU 10K				
		X76550BOLB2			0xD (SA000077K20) Micron MT41J256M16HA-093G:E	PU 10K	PD10K	PU 10K	PU 10K				
		X76550BOLB3			0x4 (SA00006E840) Hynix H5TC4G63AFR-11C	PD 10K	PD10K	PU 10K	PD 10K				

Binary [3210]	Hexadecimal	Bom
0000	0x0	
0001	0x1	1GMIC@
0010	0x2	
0011	0x3	
0100	0x4	2GAFR@
0101	0x5	
0110	0x6	
0111	0x7	
1000	0x8	
1001	0x9	2GSAM@
1010	0xA	
1011	0xB	
1100	0xC	1GFFR@
1101	0xD	2GMIC@
1110	0xE	1GSAM@
1111	0xF	

DG-06246-001_v04

Table 123 Binary Strap Mode Mapping

Strap Pin Name	Strap Mapping	Resistance	Polarity
ROM_SCLK	SMB_ALT_ADDR	10k Ω	Pull-down to GND
ROM_SI	SUB_VENDOR	10k Ω	Pull-up to 3V3 if VBIOS ROM exists Pull-down to GND if no VBIOS ROM
ROM_SO	VGA_DEVICE	10k Ω	Pull-down to GND (no display)
STRAP0	RAM_CFG[0]	10k Ω	See Note below
STRAP1	RAM_CFG[1]	10k Ω	See Note below
STRAP2	RAM_CFG[2]	10k Ω	See Note below
STRAP3	RAM_CFG[3]	10k Ω	See Note below
STRAP4	PCIE_MAX_SPEED	10k Ω	Pull-down to GND



RVL-06891-001_V05

Table 1. N15V-GM DDR3 Recommended Memories

Memory Type	FBVDD/ FBVDDQ	Memory Density	Configuration	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed CK Grade(MHz)	Memory Date Code Minimum	Status
DDR3	1.5V/ 1.5V	128Mx16	Single Rank or Single Rank Stuffing for Dual Rank	Micron	MT41J128M16JT-093G:K	K-die	0x1	1000	1234	Production ready
				Samsung	K4W2G1646E-BC1A	E-die	0x5	1000	1204	Production ready
				Hynix	H5TC2G63FFR-11C	F-die	0xC	1000	N/A	Production ready
				Samsung	K4W2G1646Q-BC1A	Q-die	0xE	1000	N/A	Production ready
		256Mx16	Single Rank or Single Rank Stuffing for Dual Rank	Hynix	H5TC4G63AFR-11C	A-die	0x4	1000	N/A	Production ready
				Micron	MT41J256M16HA-093G:E	E-die	0xD	1000	N/A	Production ready
				Samsung	K4W4G1646D-BC1A	D-die	0x9	1000	N/A	Production ready

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NV 15x DG-06803-V03

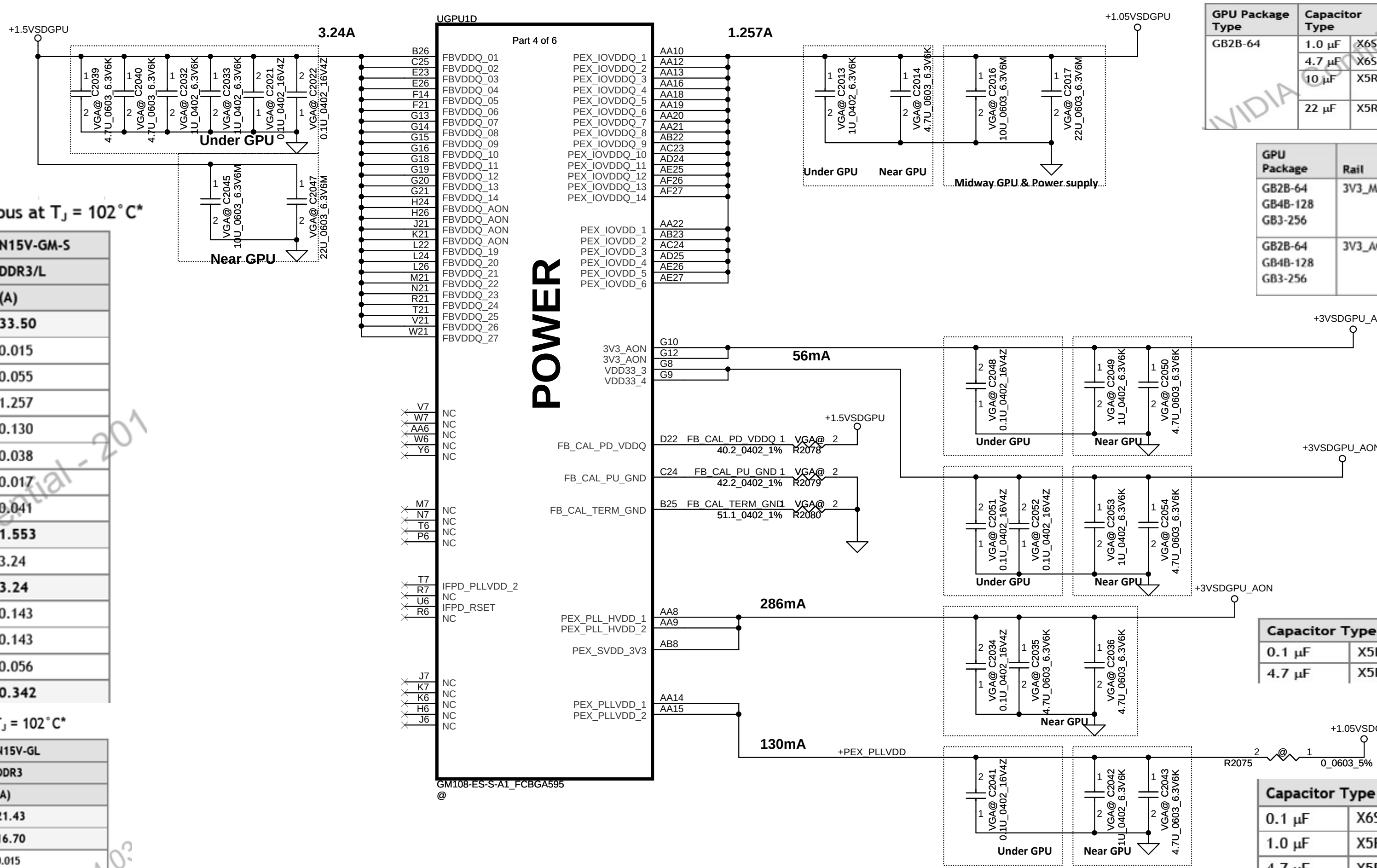
GPU Package Type	Capacitor Type		Footprint		Population	Location
GB2B-64 DDR3	0.1µF	X7R	0402	2	2	Under GPU
	1 µF	X7R	0603	2	2	Under GPU
	4.7 µF	X6S	0603	2	2	Under GPU
	10 µF	X5R	0805	1	1	Near GPU
	22 µF	X5R	0805	1	1	Near GPU

Table 2. N15V-GM DDR3L Recommended Memories

Memory Type	FBVDD/ FBVDDQ	Memory Density	Configuration	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed CK Grade(MHz)	Memory Date Code Minimum	Status
DDR3L	1.35V/ 1.35V	128Mx16	Single Rank or Single Rank Stuffing for Dual Rank	Hynix	H5TC2G63FFR-11C	F-die	0xC	900	N/A	Production ready
				Micron	MT41K128M16JT-107G:K	K-die	0x1	900	N/A	Production ready
				Samsung	K4W2G1646E-BY11	E-die	0x5	900	N/A	Production ready
				Samsung	K4W2G1646Q-BC1A	Q-die	0xE	900	N/A	Production ready
		256Mx16	Single Rank or Single Rank Stuffing for Dual Rank	Hynix	H5TC4G63AFR-11C	A-die	0x4	900	N/A	Production ready
				Micron	MT41K256M16HA-107G:E	E-die	0xD	900	N/A	Production ready
				Samsung	K4W4G1646D-BC1A	D-die	0x9	900	N/A	Post-production candidate

GPU Package Type	Capacitor Type		Footprint	Population	Location
GB2B-64	1.0 µF	X6S	0402	1	Under GPU
	4.7 µF	X6S	0603	1	Near GPU
	10 µF	X5R	0805	1	Midway between GPU and Power Supply
	22 µF	X5R	0805	1	Midway between GPU and Power Supply

GPU Package	Rail	Capacitor Type		Footprint		Population	Location
GB2B-64 GB4B-128 GB3-256	3V3_MAIN	0.1µF	X6S	0402	2	2	Under GPU
		1 µF	X5R	0603	1	1	Near GPU
		4.7 µF	X5R	0603	1	1	Near GPU
GB2B-64 GB4B-128 GB3-256	3V3_AON	0.1µF	X6S	0402	1	1	Under GPU
		1 µF	X5R	0603	1	1	Near GPU
		4.7 µF	X5R	0603	1	1	Near GPU



DA-06925-001_v05_secured

Table 5. EDP-Continuous at T_J = 102˚C*

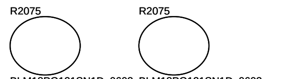
Power Supply Rail		N15V-GM-S
		DDR3/L
	(V)	(A)
GPU Core Max	-	33.50
FB_DLLAVDD	1.05	0.015
FBA_PLLAVDD	1.05	0.055
PEX_IOVDD/Q	1.05	1.257
PEX_PLLVDD	1.05	0.130
PLLVDD	1.05	0.038
SP_PLLVDD	1.05	0.017
VID_PLLVDD	1.05	0.041
TOTAL	1.05	1.553
FB Total	1.5/1.35	3.24
TOTAL	1.5/1.35	3.24
PEX_SVDD_3v3	3.3	0.143
PEX_PLL_HVDD	3.3	0.143
VDD33	3.3	0.056
TOTAL	3.3	0.342

Table 6. EDP-Continuous at T_J = 102˚C*

Power Supply Rail		N15V-GL
		DDR3
	(V)	(A)
GPU Core Max	-	21.43
GPU Core Rated	-	16.70
FB_DLLAVDD	1.05	0.015
FBA_PLLAVDD	1.05	0.055
PEX_IOVDD/Q	1.05	0.855
PEX_PLLVDD	1.05	0.130
PLLVDD	1.05	0.038
SP_PLLVDD	1.05	0.017
VID_PLLVDD	1.05	0.041
TOTAL	1.05	1.151
FB Total	1.5	2.97
TOTAL	1.5	2.97
PEX_SVDD_3v3	3.3	0.143
PEX_PLL_HVDD	3.3	0.143
VDD33	3.3	0.056
TOTAL	3.3	0.342

Capacitor Type		Footprint	Population	Location
0.1 µF	X5R	0402	1	Near GPU
4.7 µF	X5R	0603	2	Near GPU

Capacitor Type		Footprint	Population	Location
0.1 µF	X6S	0402	1	Under GPU
1.0 µF	X5R	0603	1	Near GPU
4.7 µF	X5R	0805	1	Near GPU



BLM18PG121SN1D_0603 VGL@ SM01000BW00

BLM18PG121SN1D_0603 VGM@ SM01000BW00

SM010028800 2000ma 120ohm@100mhz DCR 0.1

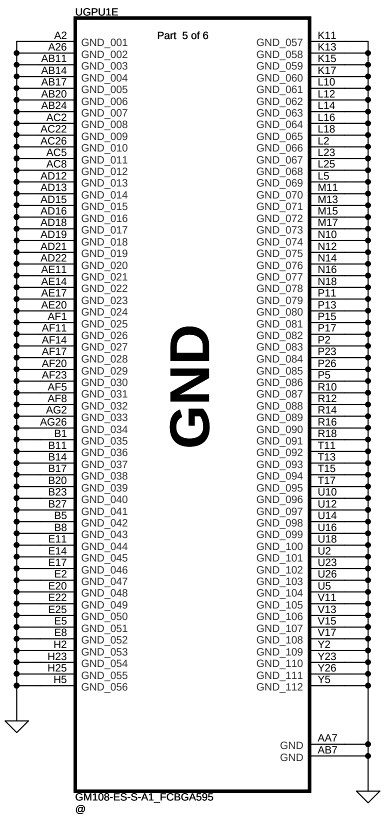
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Issued Date	2014/03/19	Deciphered Date	2015/03/18

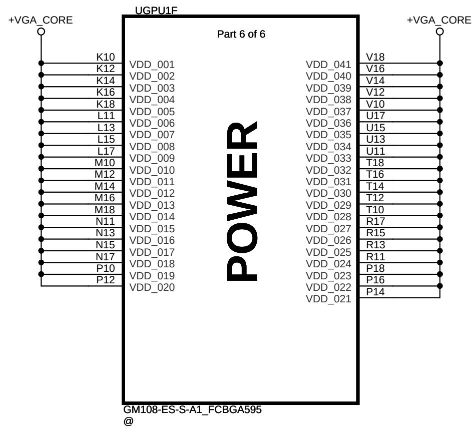
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NV 15x DG-06803-V03

GPU Package Type	Capacitor Type		Footprint		Population	Location	Comments
GB2B-64	4.7 μF	X6S	0603	10	10	Under GPU	
	1 μF	X6S	0402	4	4	Under GPU	
	47 μF	X5R	0805	1	1	Near GPU	
	22 μF	X5R	0805	1	1	Near GPU	
	4.7 μF	X5R	0805	5	5	Near GPU	
	330 μF	POS	7343	1	1	Near GPU	ESR ≤ 6 mΩ

DA-06925-V05

Table 6. EDP-Peak at T_J = 102˚C

Power Supply Rail	N15V-GM-S
	DDR3/L
(V)	(A)
GPU Core Max	51.50
FB Total	4.25
PEXVDD	2.29

DA07075-V01

Table 7. EDP-Peak at T_J = 102˚C

Power Supply Rail	N15V-GL
	DDR3
(V)	(A)
GPU Core Max	28.26
FB Total	4.07
PEXVDD	1.82

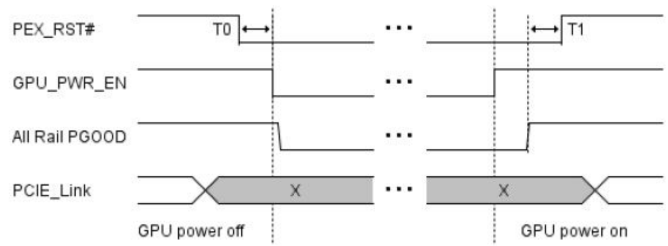


Figure 18-7. Optimus Entry/Exit Timing Diagram

Table 18-1. Optimus Timing Parameters

Symbol	Description	Min	Max	Units
T0	PEX_RST# assertion to GPU_PWR_EN=0	>0	5	ms
T1	All GPU power rail up and stable to PEX_RST# de-assertion	0.1	5	ms



Notes: - All 3.3V includes all rails powered at 3.3V
- PEX_VDD 1.05V includes all rails that are shared

Figure 3-6. Example of Power-up Sequencing Order

Note:

- The ramp time for any rail must be more than 40 μs and is recommended to be less than 2ms.

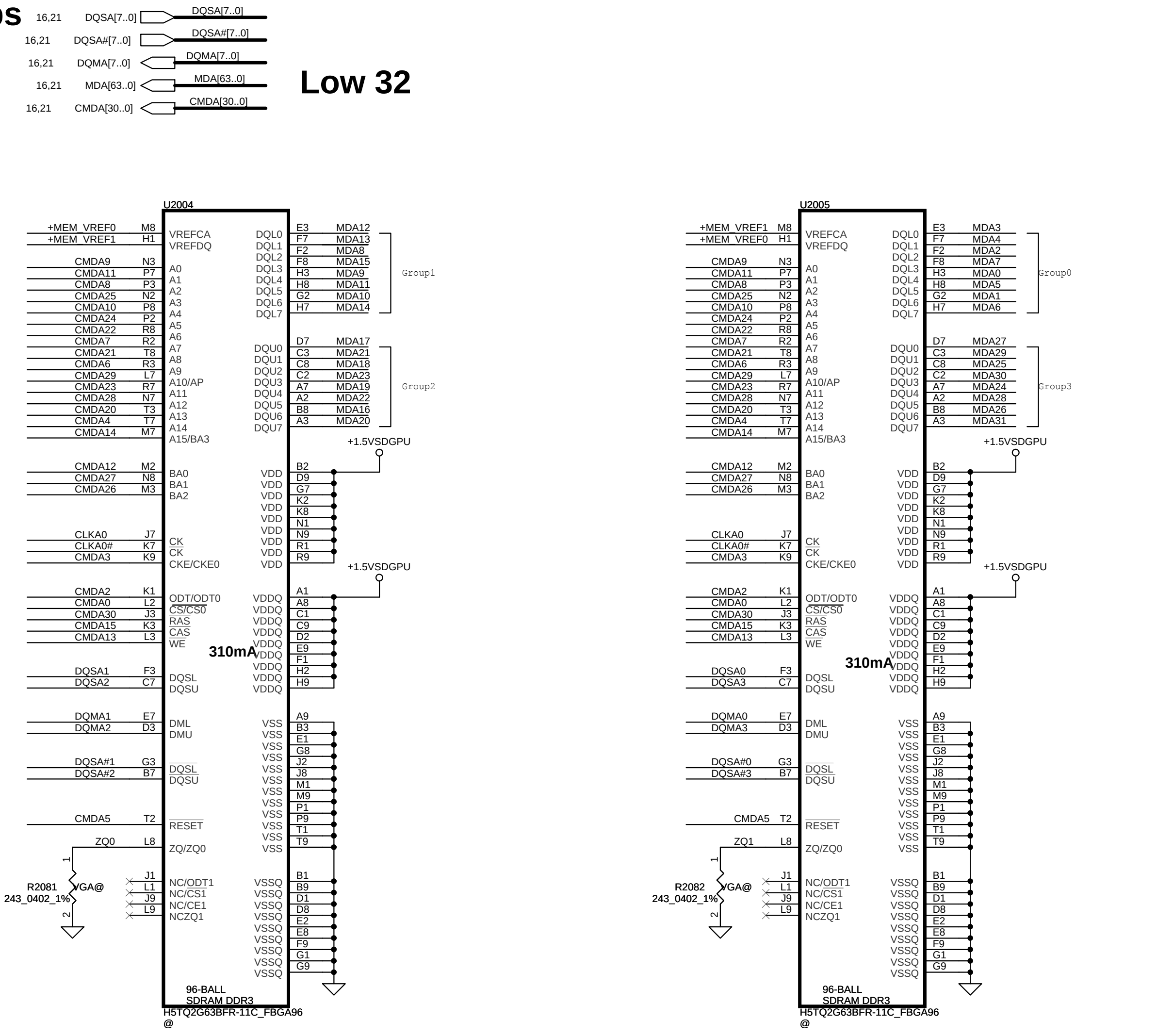
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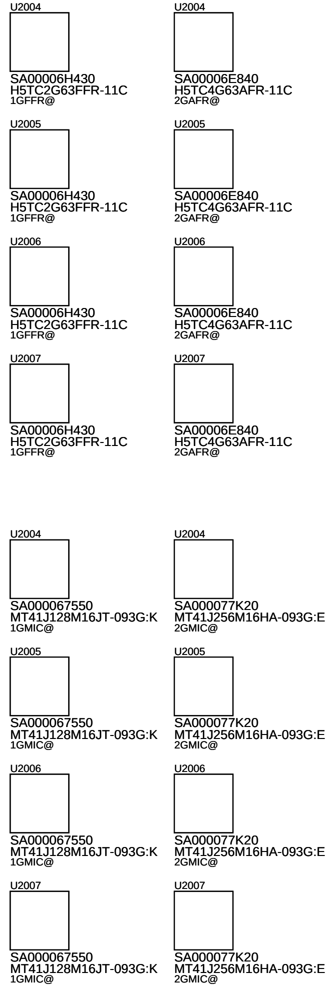
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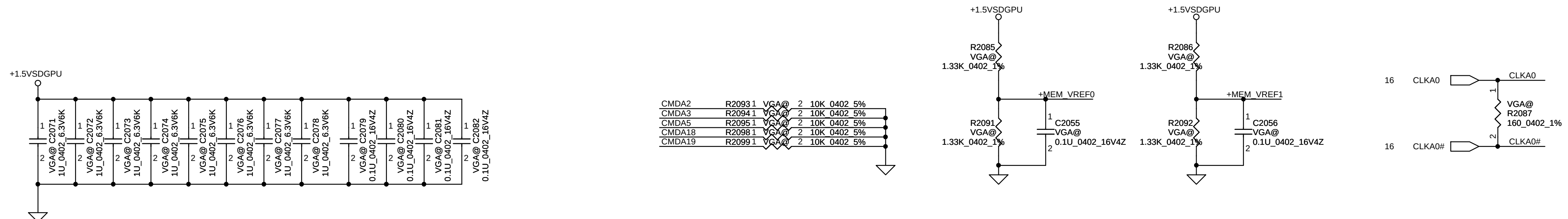
VRAM DDR3 chips



Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE_L	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination





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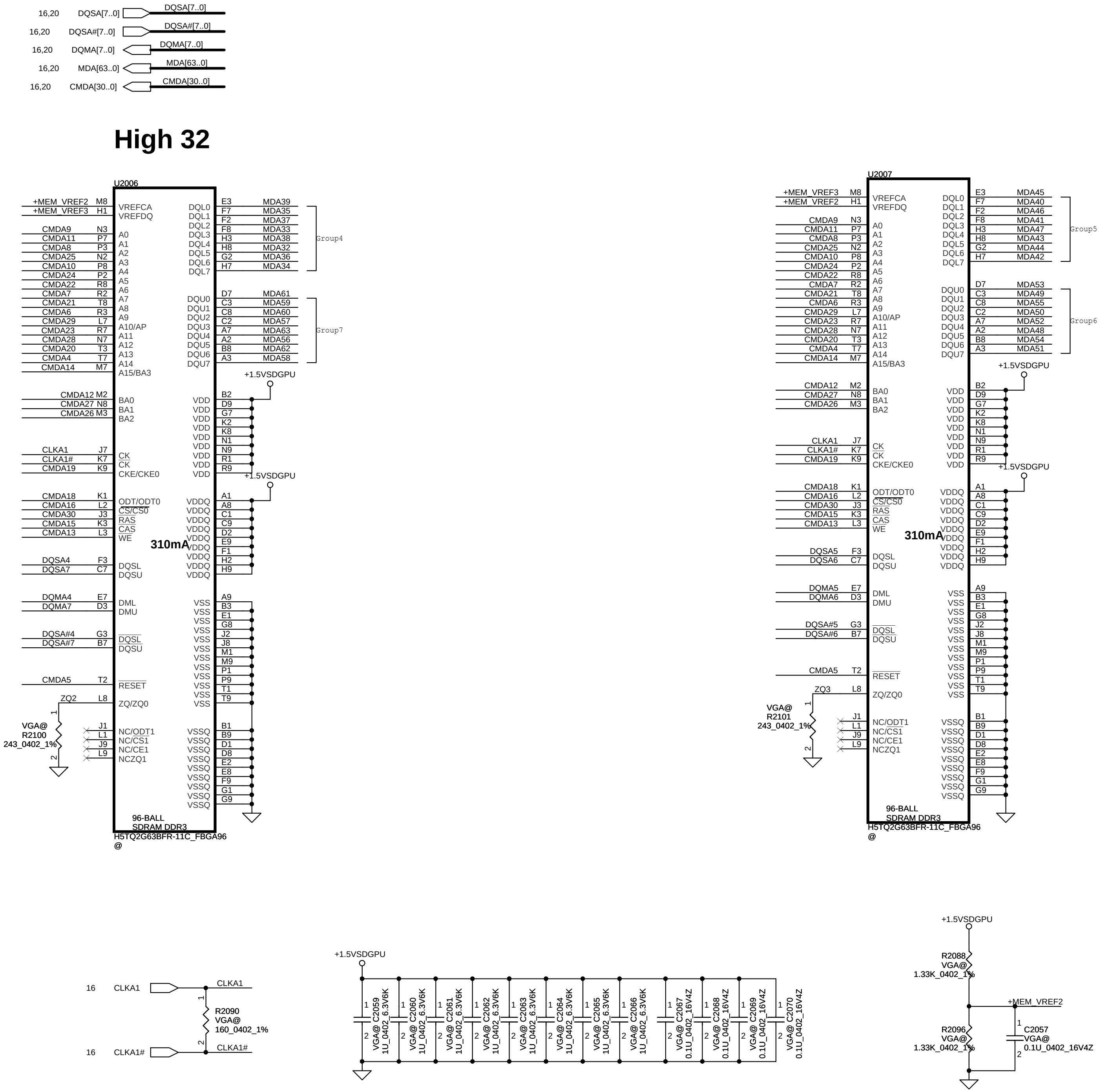
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VRAM DDR3 chips



Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE_L	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination

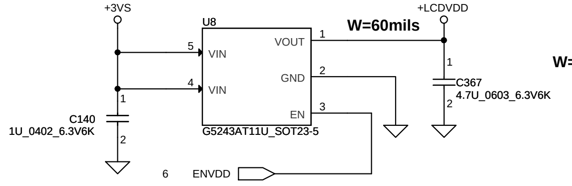
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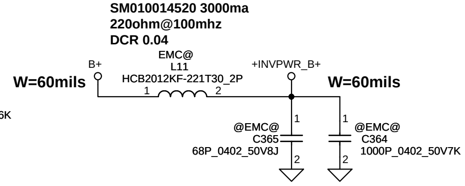
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Title: N15X DDR3 7/7

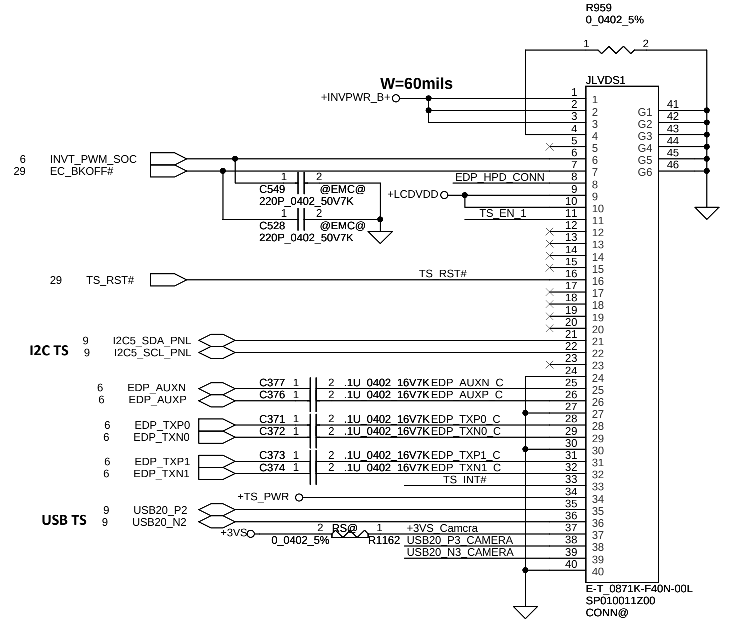
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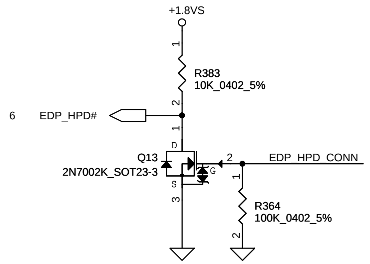
LCD POWER CIRCUIT

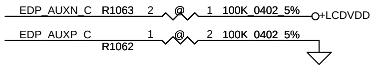




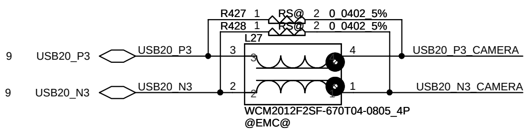
LCD/ LED PANEL Conn.



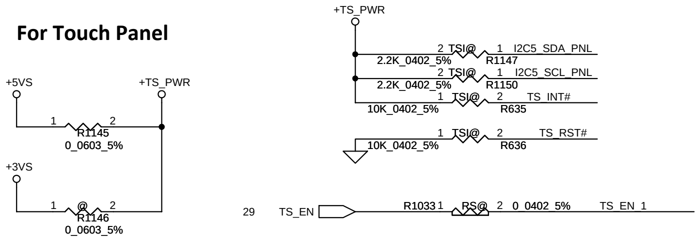


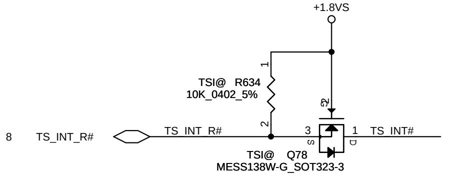


Intel recommends having a pull-up resistor of 100 kΩ for AUXN and a pull-down resistor of 100 kΩ for AUXP between the AC capacitor and the connector, to assist source detection by the sink device.

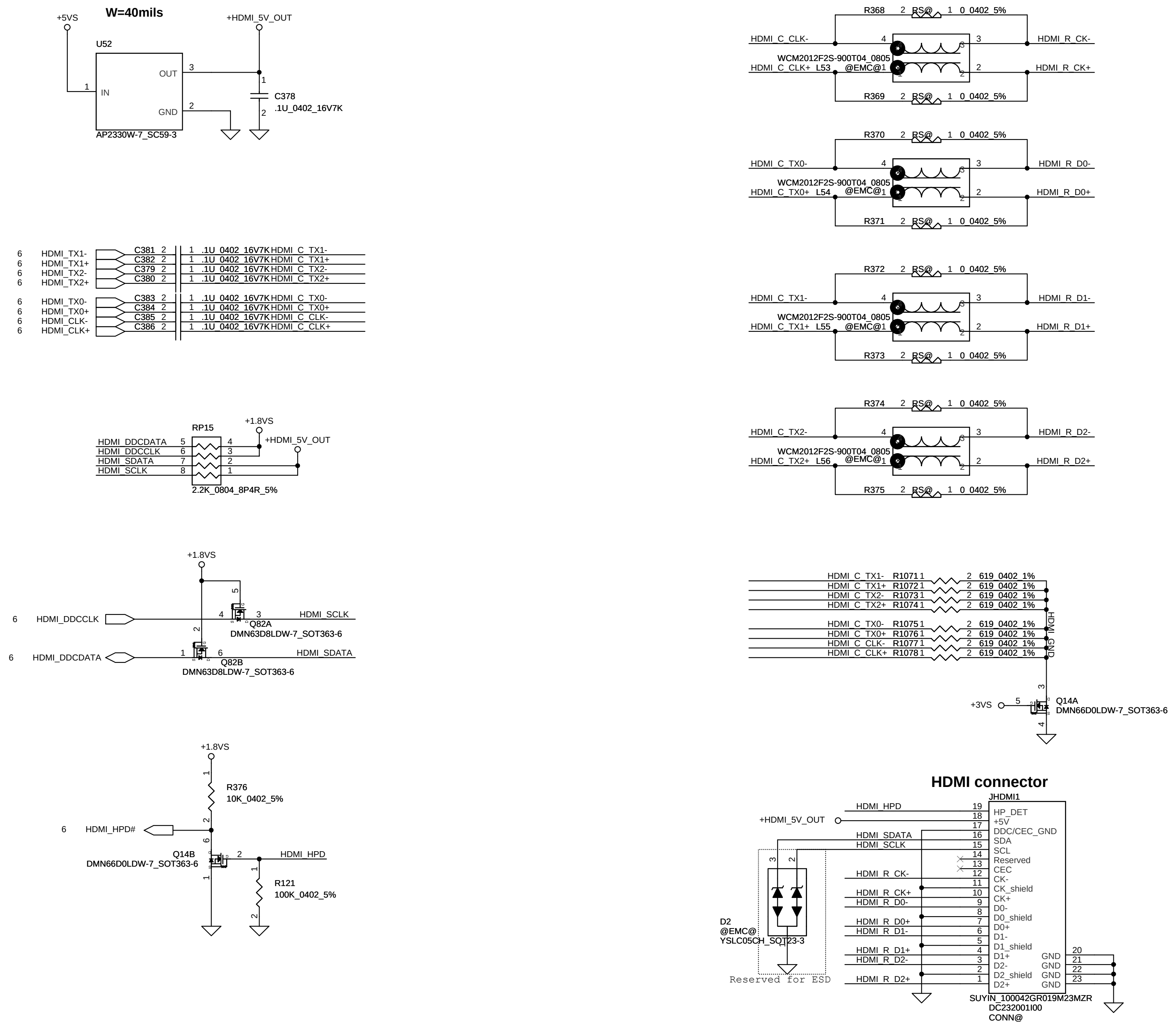


For Touch Panel

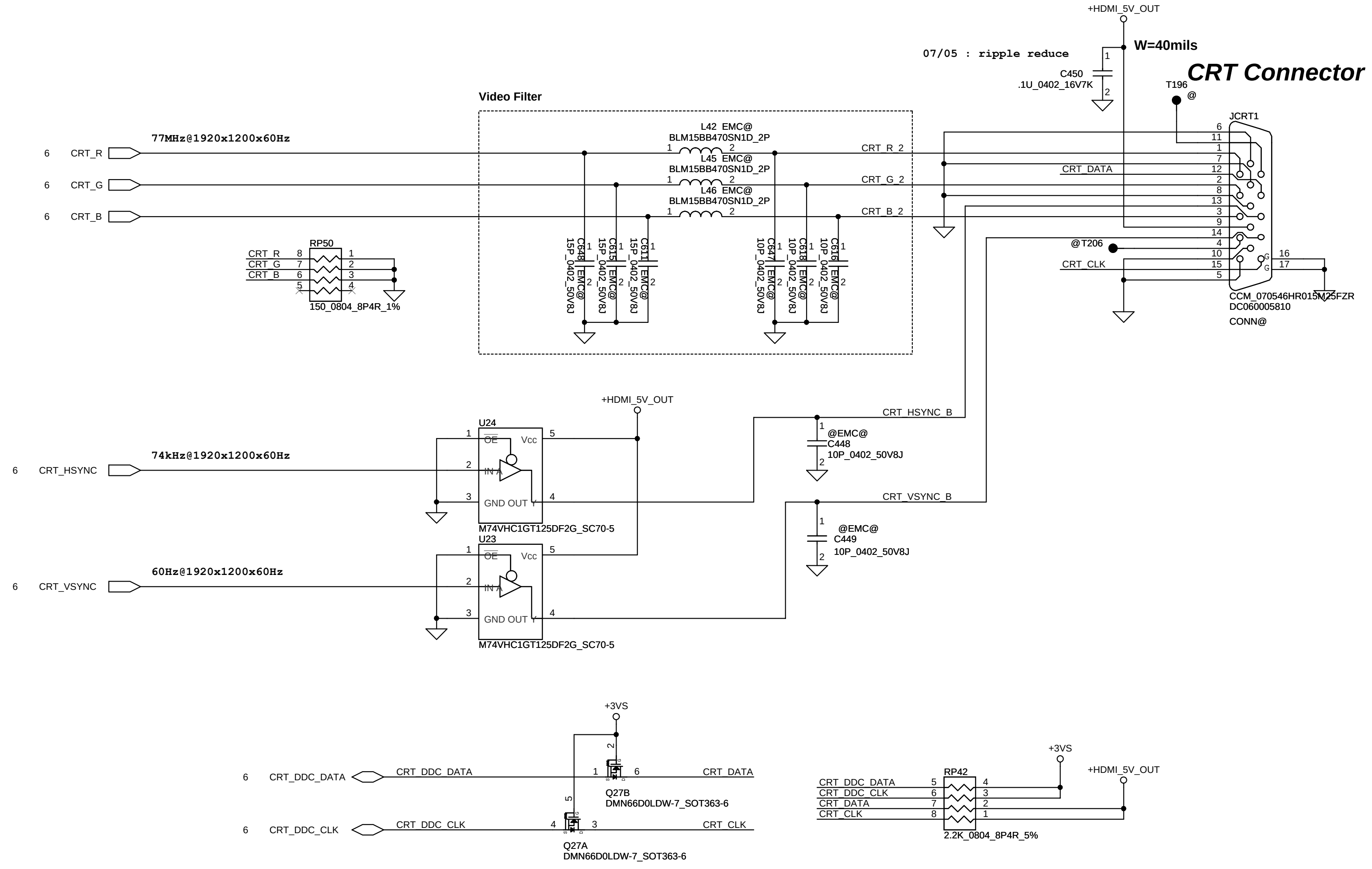




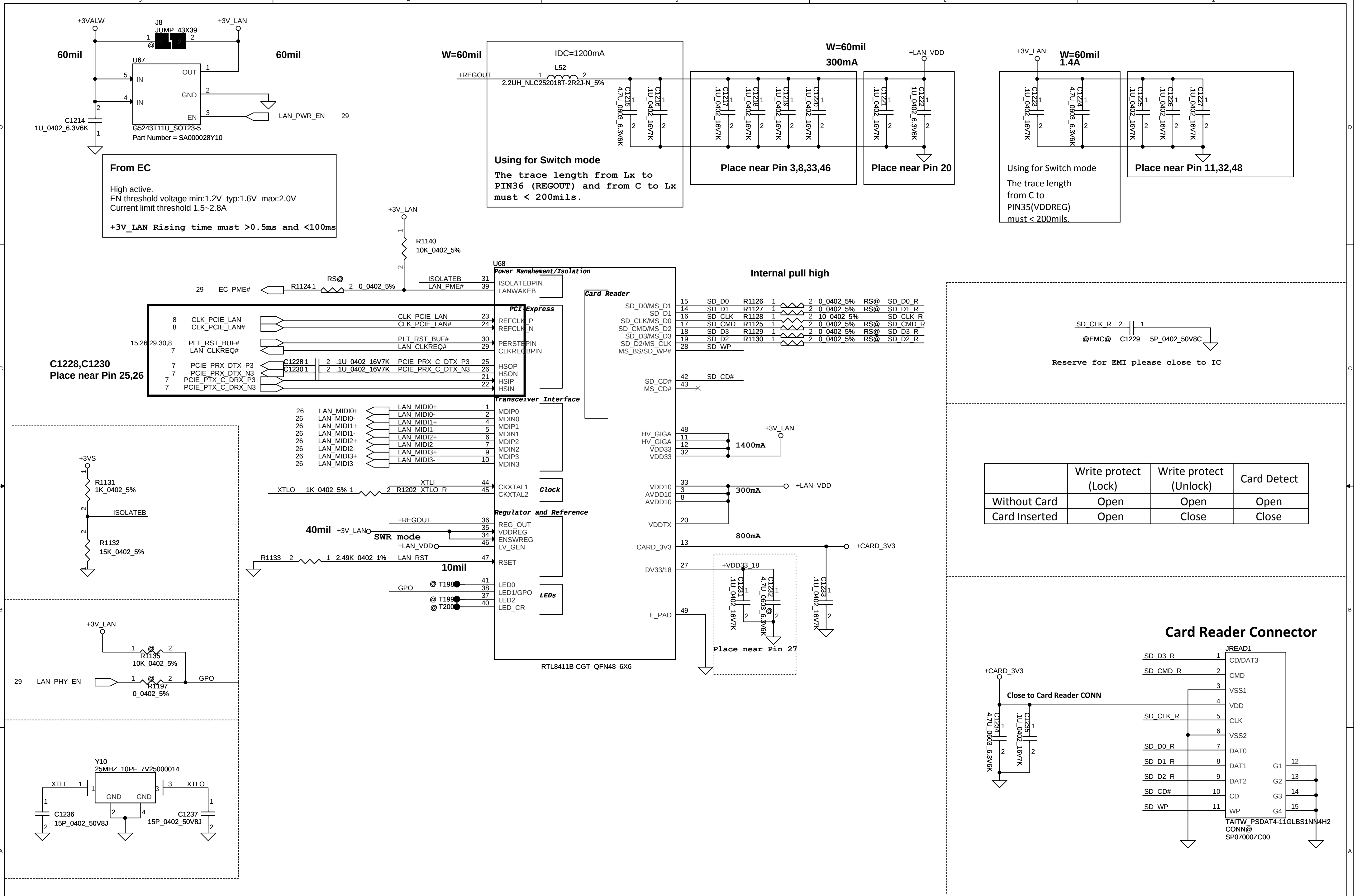
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	Write protect (Lock)	Write protect (Unlock)	Card Detect
Without Card	Open	Open	Open
Card Inserted	Open	Close	Close

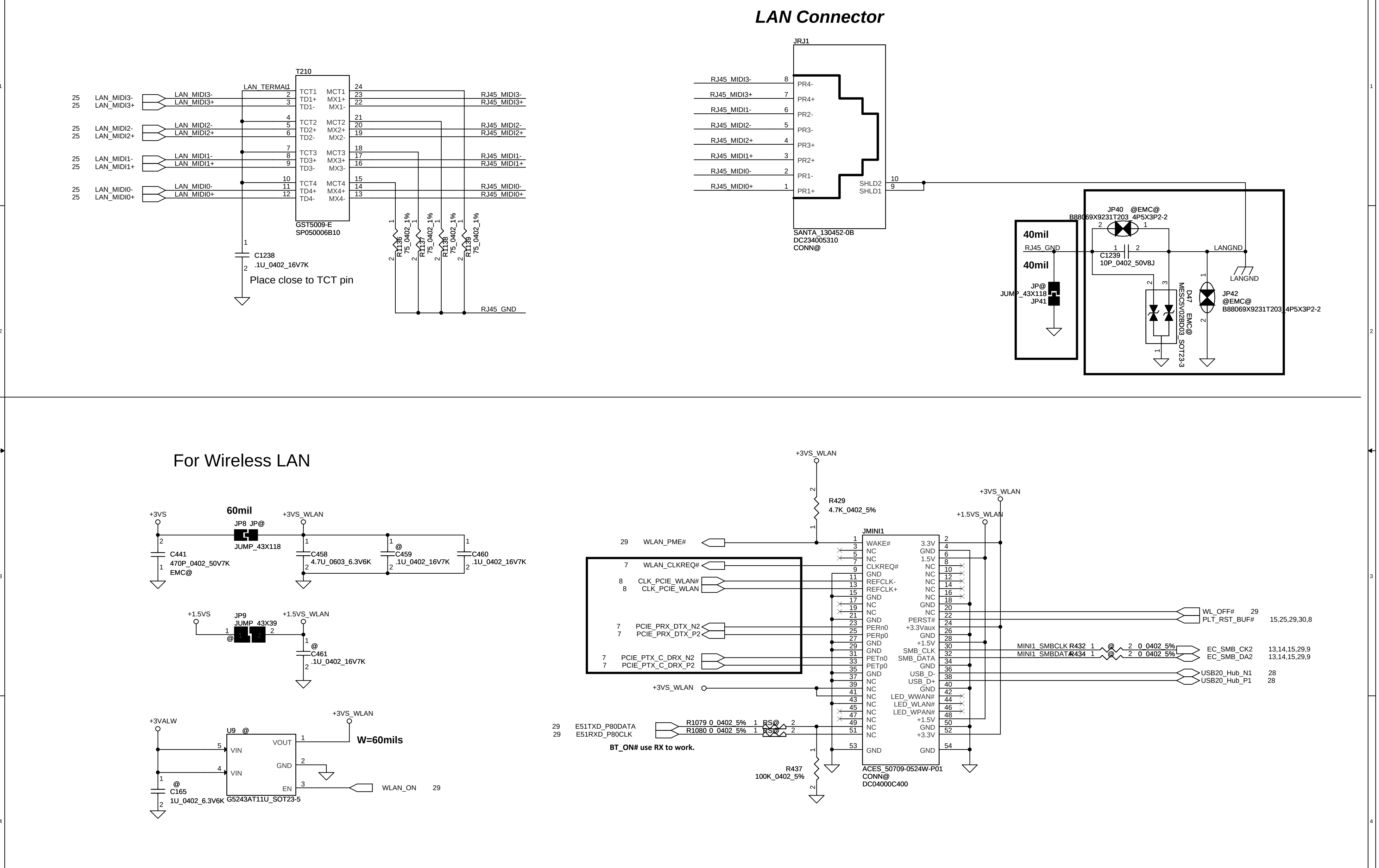
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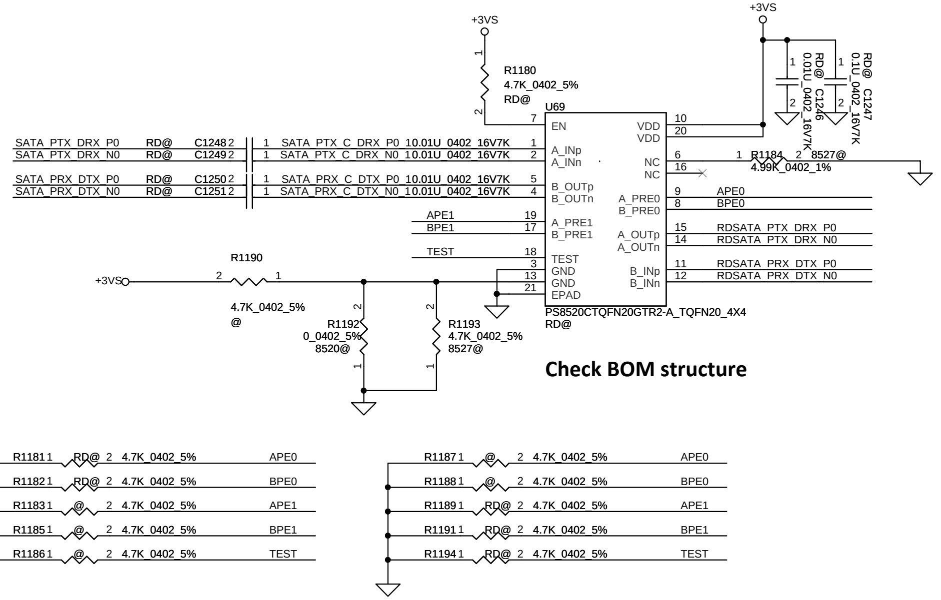
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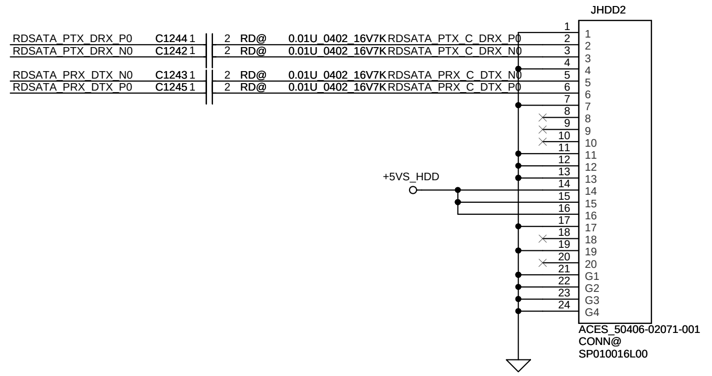
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SATA Re-Driver HDD2 Conn. Reserve

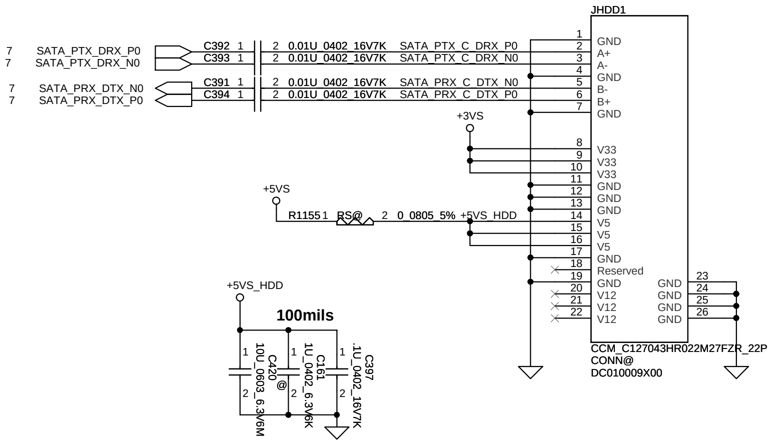


SATA HDD2 Cable Conn.

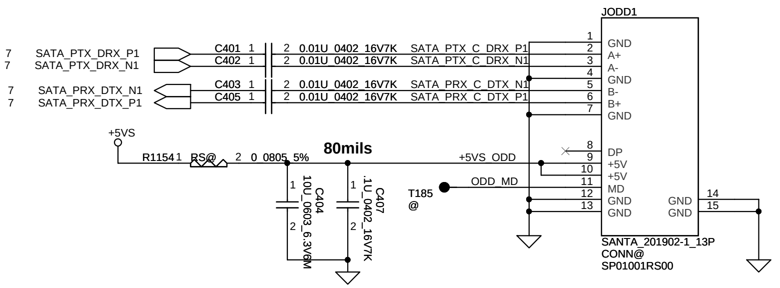
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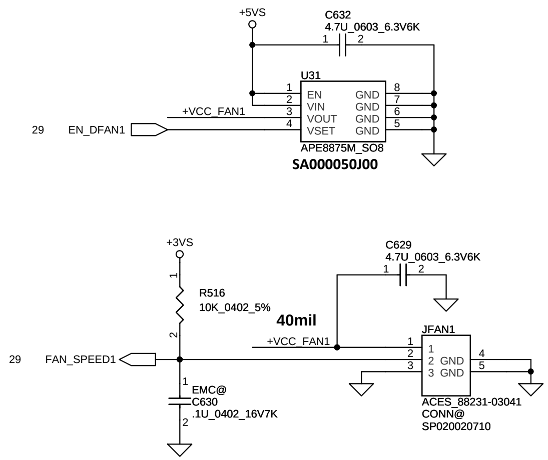
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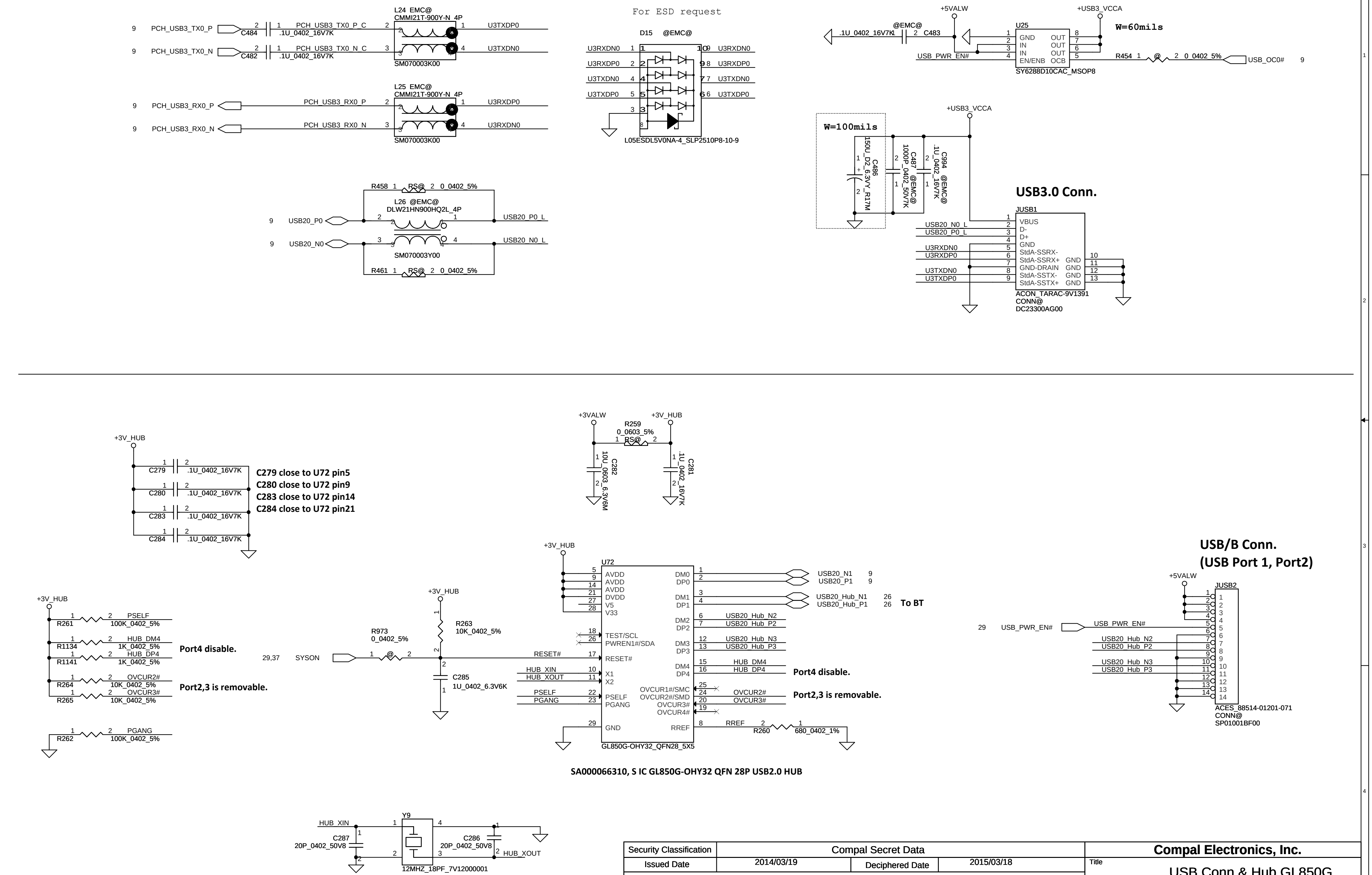
SATA ODD Conn.



FAN1 Conn



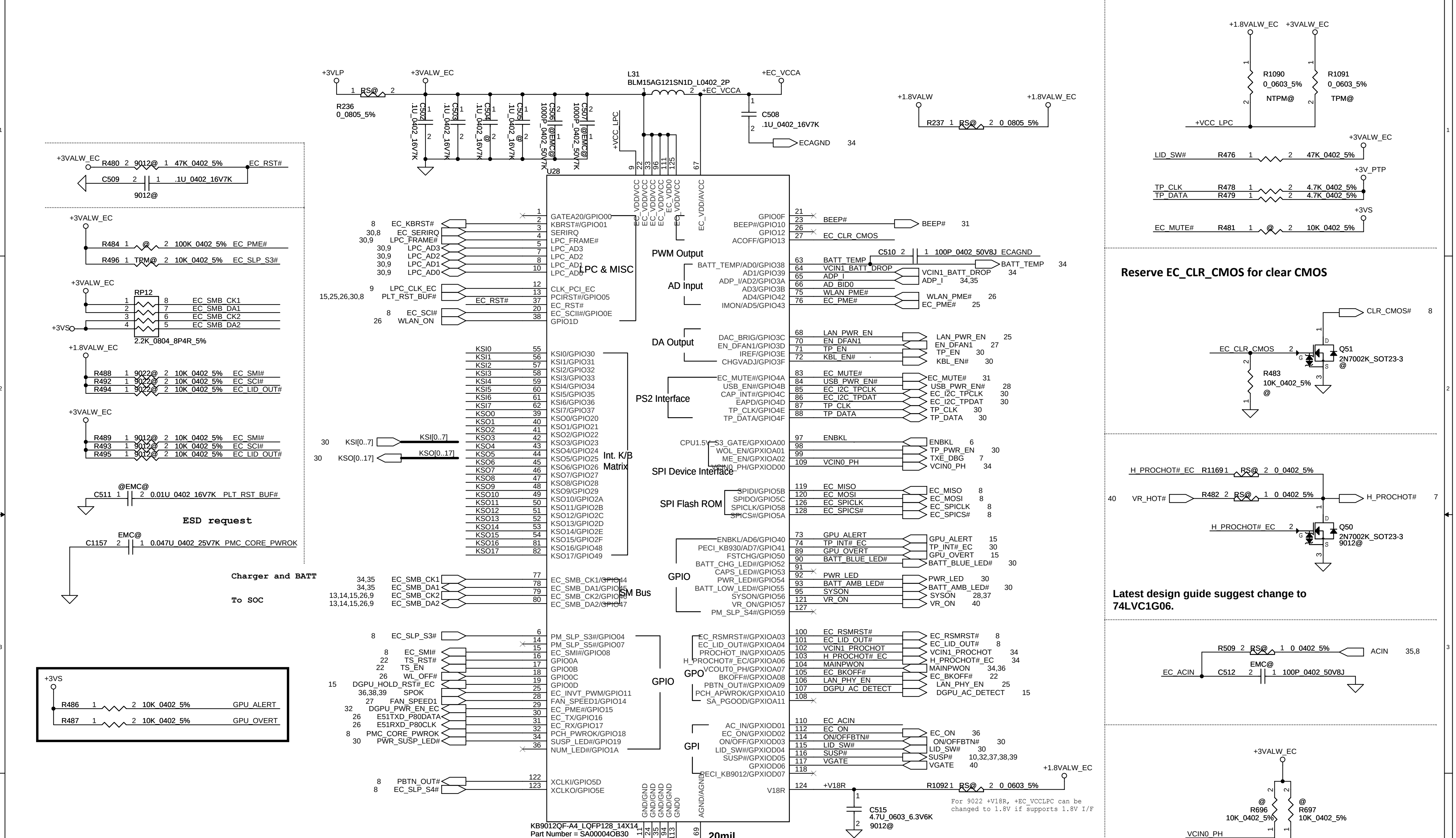
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Board ID

Analog Board ID definition, Please see page 3.

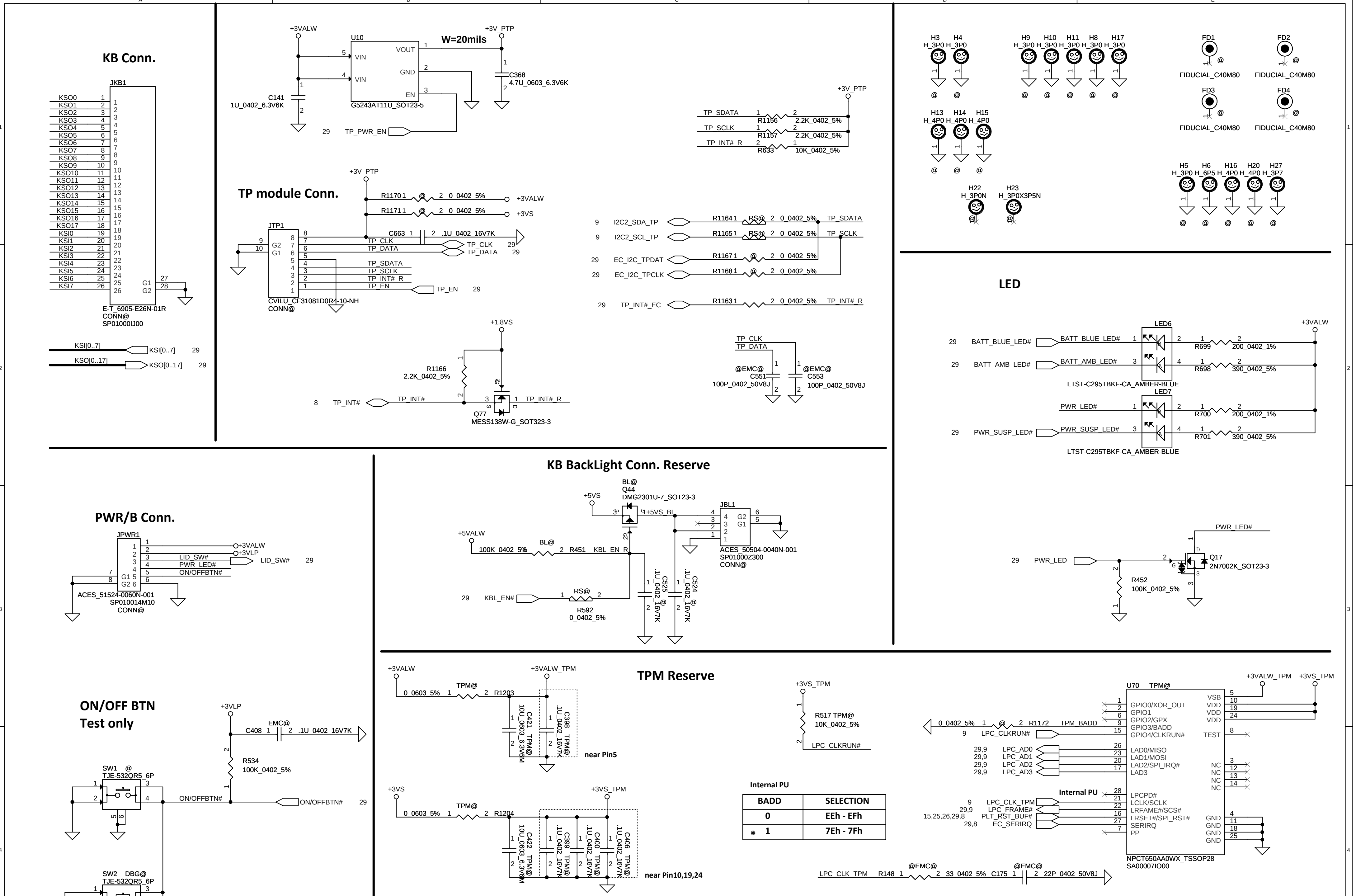
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* PVT	0.2	11

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Internal PU

BADD	SELECTION
0	EEh - EFh
* 1	7Eh - 7Fh

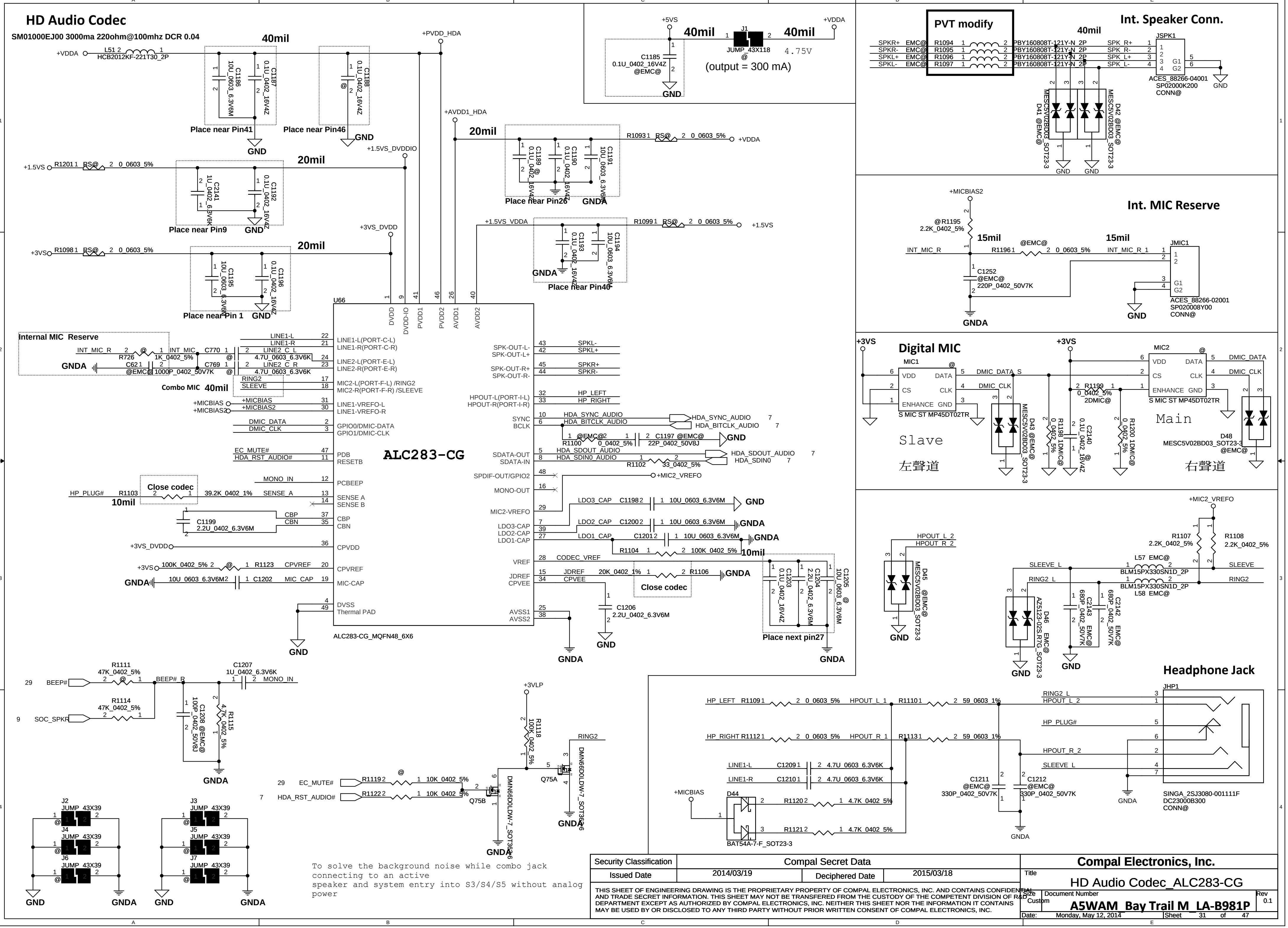
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Title: KB/TP/LED/TPM/Screw Hole

Size: Custom | Document Number: A5WAM_Bay Trail M_LA-B981P | Rev: 0.1

Date: Monday, May 12, 2014 | Sheet 30 of 47



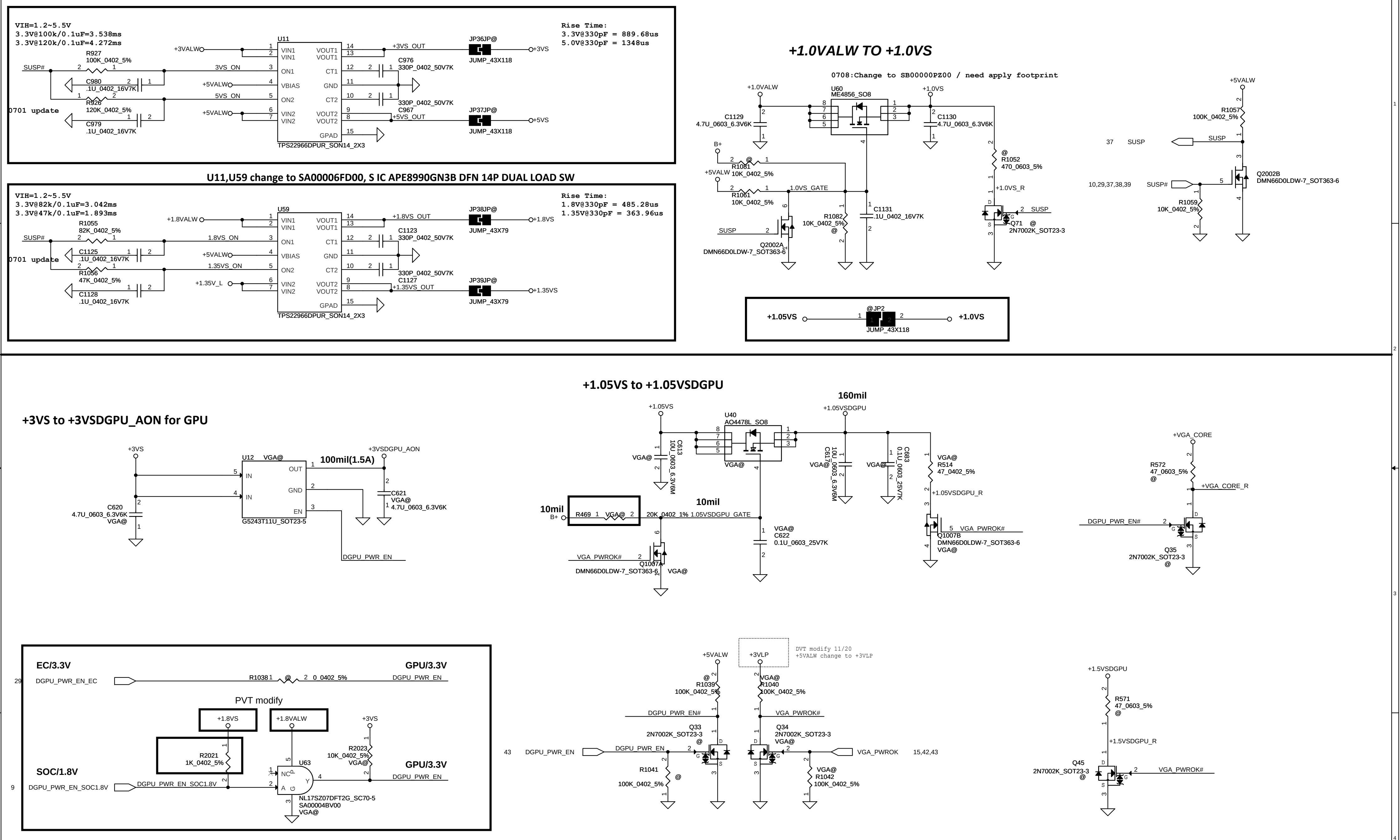
To solve the background noise while combo jack connecting to an active speaker and system entry into S3/S4/S5 without analog power

Security Classification	Compal Secret Data		
Issued Date	2014/03/19	Deciphered Date	2015/03/18

Compal Electronics, Inc.

Title: HD Audio Codec_ALC283-CG

Size: Custom | Document Number: A5WAM_Bay Trail M_LA-B981P | Rev: 0.1



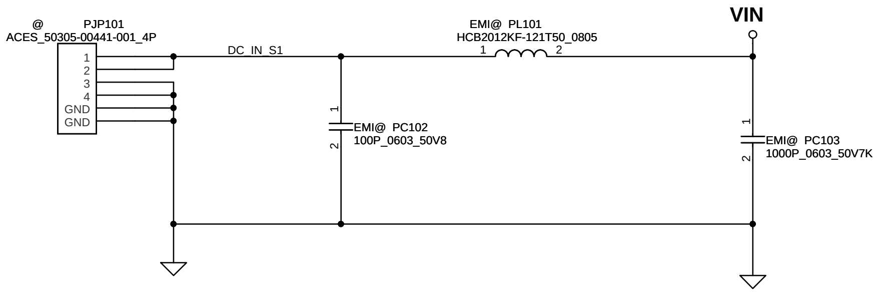
Security Classification	Compal Secret Data		
Issued Date	2014/03/19	Deciphered Date	2015/03/18

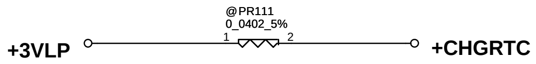
Compal Electronics, Inc.

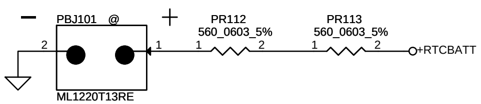
Title: DC INTERFACE

Size: Custom | Document Number: A5WAM_Bay Trail M_LA-B981P | Rev: 0.1

Date: Monday, May 12, 2014 | Sheet 32 of 47



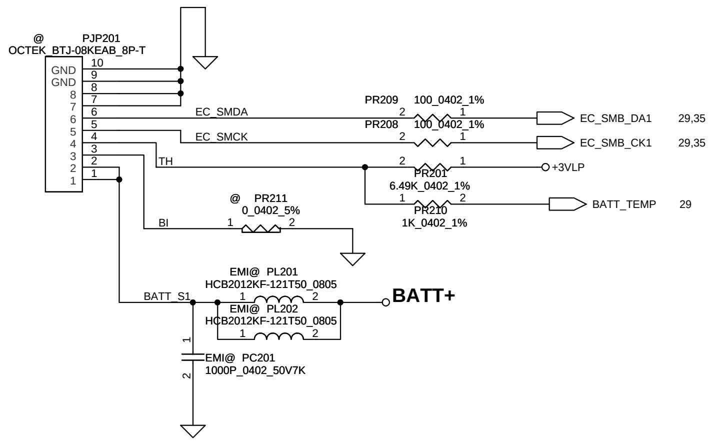


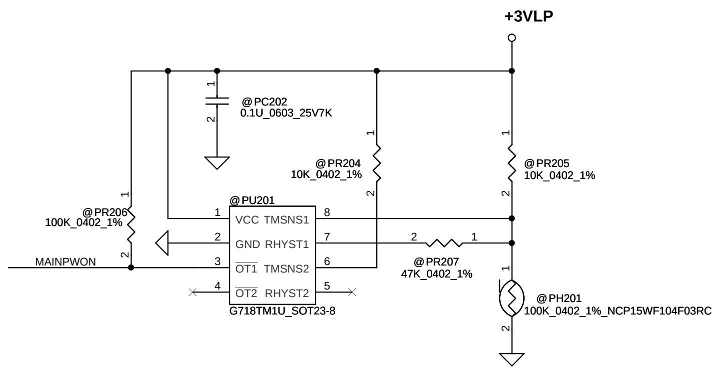


Security Classification	Compal Secret Data		
Issued Date	2014/03/19	Deciphered Date	2015/03/18

Compal Electronics, Inc.

Title	DCIN / RTC	
Size: Custom	Document Number: A5WAM_Bay Trail M_LA-B981P	Rev: 0.1
Date: Monday, May 12, 2014	Sheet 33 of 47	





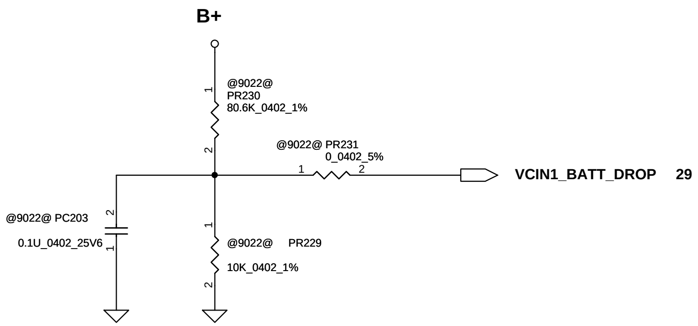
---Battery_pin define---
PIN1 GND
PIN2 GND
PIN3 SMD
PIN4 SMC
PIN5 TS
PIN6 B/I
PIN7 Batt+
PIN8 Batt+

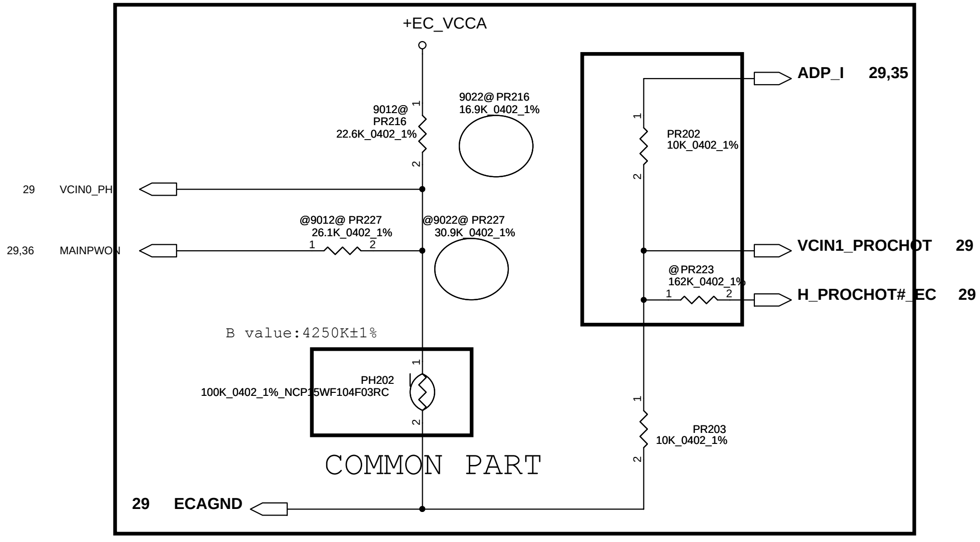
---Battery Con_pin define---
PIN8 GND
PIN7 GND
PIN6 SMD
PIN5 SMC
PIN4 TS
PIN3 B/I
PIN2 Batt+
PIN1 Batt+

	For KB9012 OTP	For KB9022 OTP
92℃	1.2V	1.0V
56℃	1.2V	1.0V
PR216	22.6K ohm	32.4K ohm
PR227	26.1K ohm	30.9K ohm

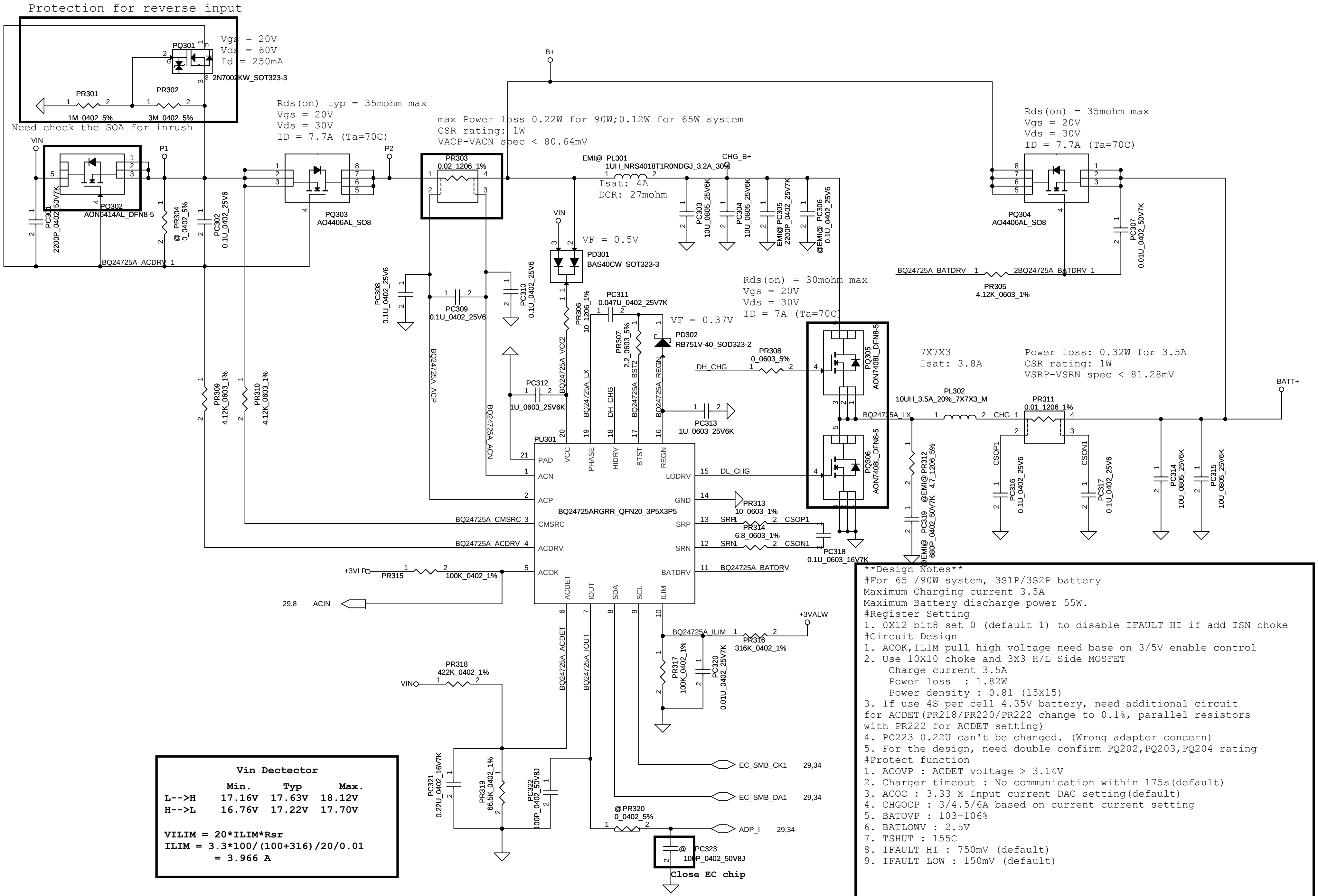
Need confirm the setting

For KB9012 sense 10mΩ	Active	Recovery
65W	69.55W,0.73V	55.9W,0.59V
40W	42.8W,0.73V	34.4W,0.59V





Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2014/03/19	Deciphered Date	2015/03/18	Title: BATTERY CONN / OTP
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				Date: Monday, May 12, 2014; Sheet 34 of 47

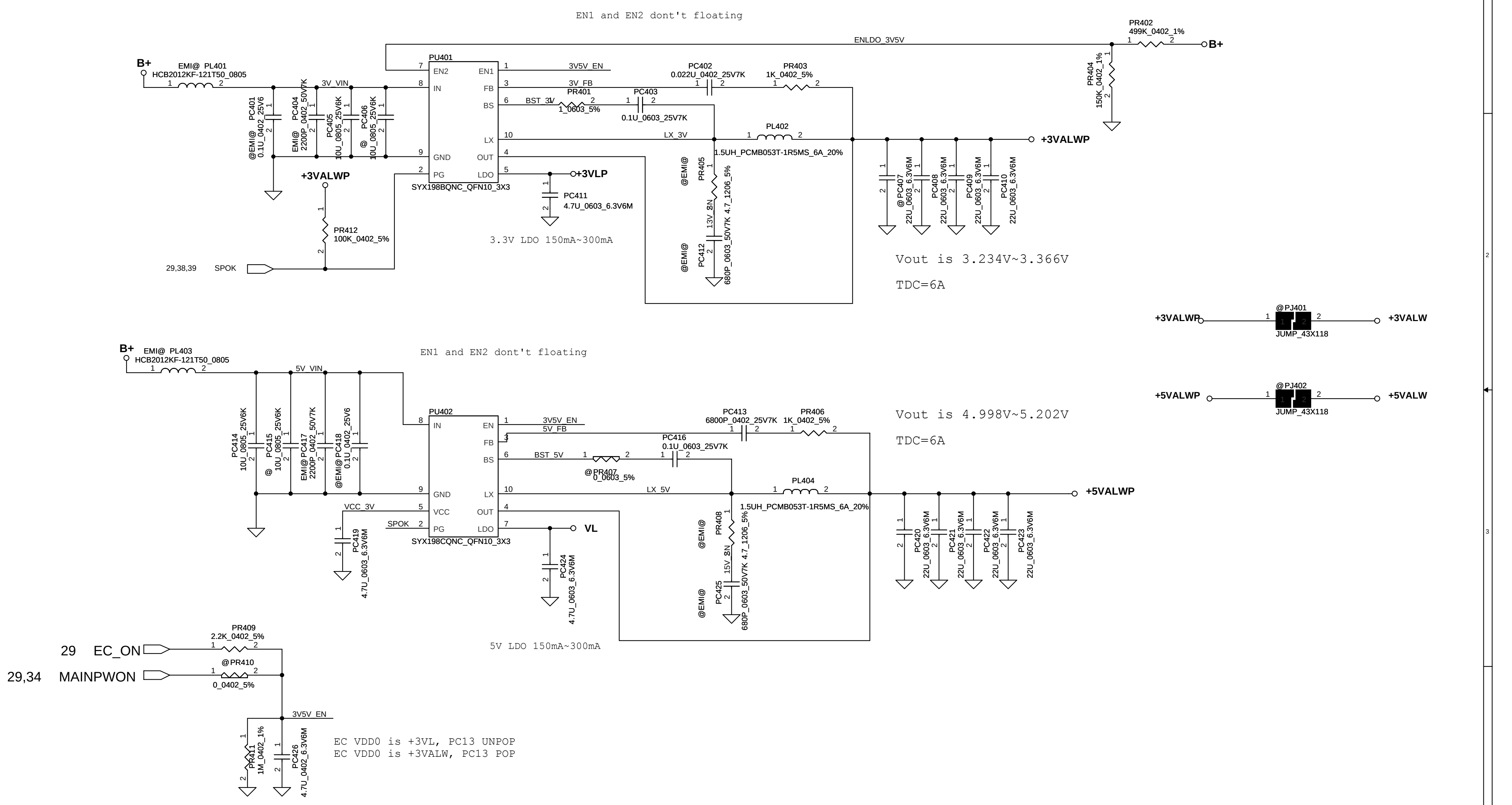


Vin Dectector

	Min.	Typ	Max.
L-->H	17.16V	17.63V	18.12V
H-->L	16.76V	17.22V	17.70V

VILIM = 20*ILIM*Rsr
ILIM = 3.3*100/(100+316)/20/0.01
= 3.966 A

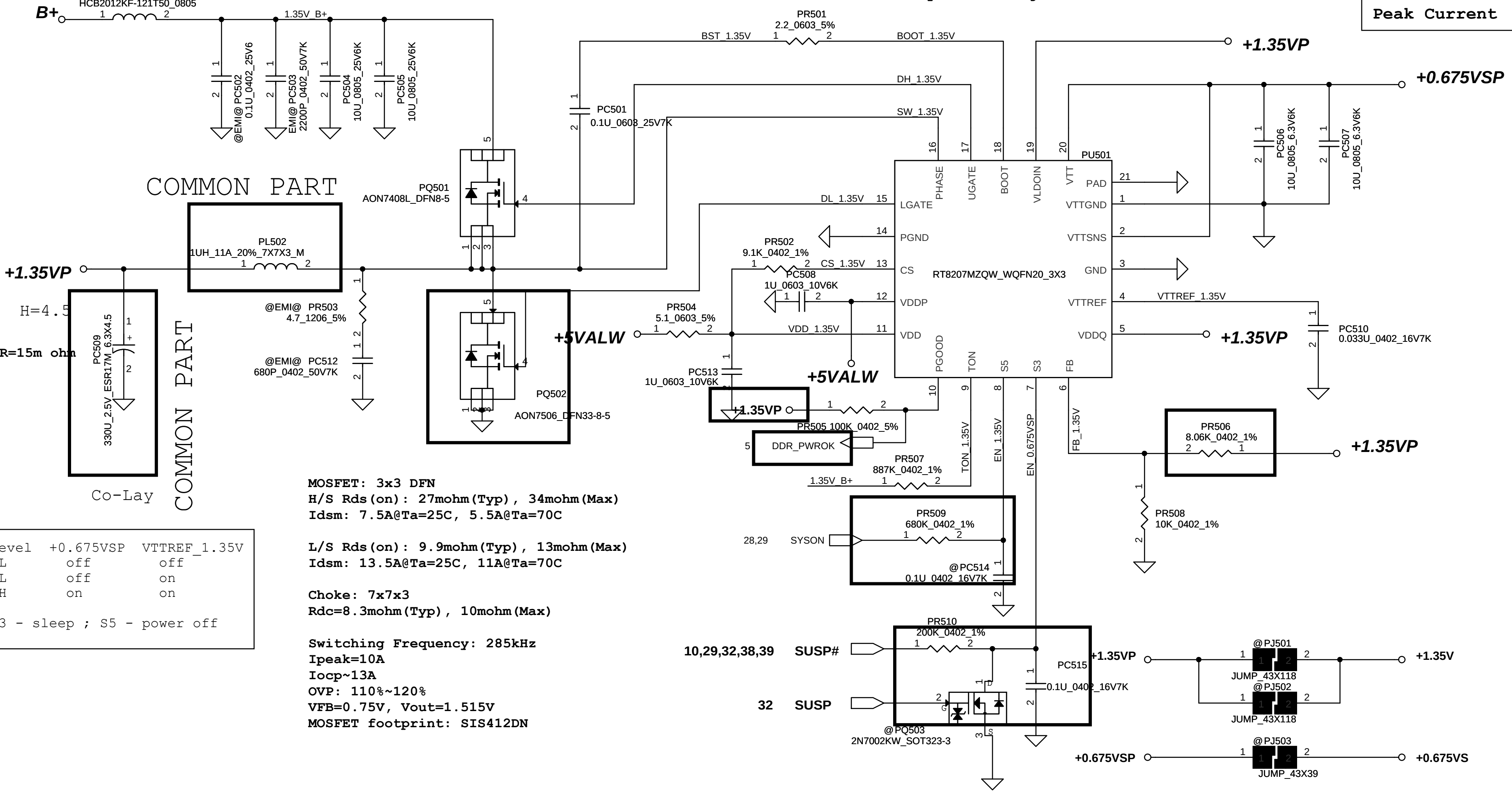
Design Notes
#For 65 /90W system, 3S1P/3S2P battery
Maximum Charging current 3.5A
Maximum Battery discharge power 55W.
#Register Setting
1. 0X12 bit8 set 0 (default 1) to disable IFAULT HI if add ISN choke
#Circuit Design
1. ACOK,ILIM pull high voltage need base on 3/5V enable control
2. Use 10X10 choke and 3X3 H/L Side MOSFET
   Charge current 3.5A
   Power loss : 1.82W
   Power density : 0.81 (15X15)
3. If use 4S per cell 4.35V battery, need additional circuit for ACDET(PR218/PR220/PR222 change to 0.1%, parallel resistors with PR222 for ACDET setting)
4. PC223 0.22U can't be changed. (Wrong adapter concern)
5. For the design, need double confirm PQ202,PQ203,PQ204 rating
#Protect function
1. ACOVP : ACDET voltage > 3.14V
2. Charger timeout : No communication within 175s(default)
3. ACOC : 3.33 X Input current DAC setting(default)
4. CHGOCP : 3/4.5/6A based on current current setting
5. BATOVP : 103-106%
6. BATLOWV : 2.5V
7. TSHUT : 155C
8. IFAULT HI : 750mV (default)
9. IFAULT LOW : 150mV (default)



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2014/03/19	Deciphered Date	2015/03/18	Title: 3VALW/5VALW
Size: Custom	Document Number: A5WAM_Bay Trail M_LA-B981P			Rev: 0.1
Date: Monday, May 12, 2014	Sheet 36 of 47			

Pin19 need pull separate from +1.35VP.
If you have +1.35V and +0.675V sequence question,
you can change from +1.35VP to +1.35VS.

0.675Volt +/- 5%
TDC 0.84A
Peak Current 1.2A



MOSFET: 3x3 DFN
H/S Rds(on): 27mohm(Typ), 34mohm(Max)
Idsm: 7.5A@Ta=25C, 5.5A@Ta=70C

L/S Rds(on): 9.9mohm(Typ), 13mohm(Max)
Idsm: 13.5A@Ta=25C, 11A@Ta=70C

Choke: 7x7x3
Rdc=8.3mohm(Typ), 10mohm(Max)

Switching Frequency: 285kHz
Ipeak=10A
Iocp~13A
OVP: 110%~120%
VFB=0.75V, Vout=1.515V
MOSFET footprint: SIS412DN

Mode	Level	+0.675VSP	VTTREF_1.35V
S5	L	off	off
S3	L	off	on
S0	H	on	on

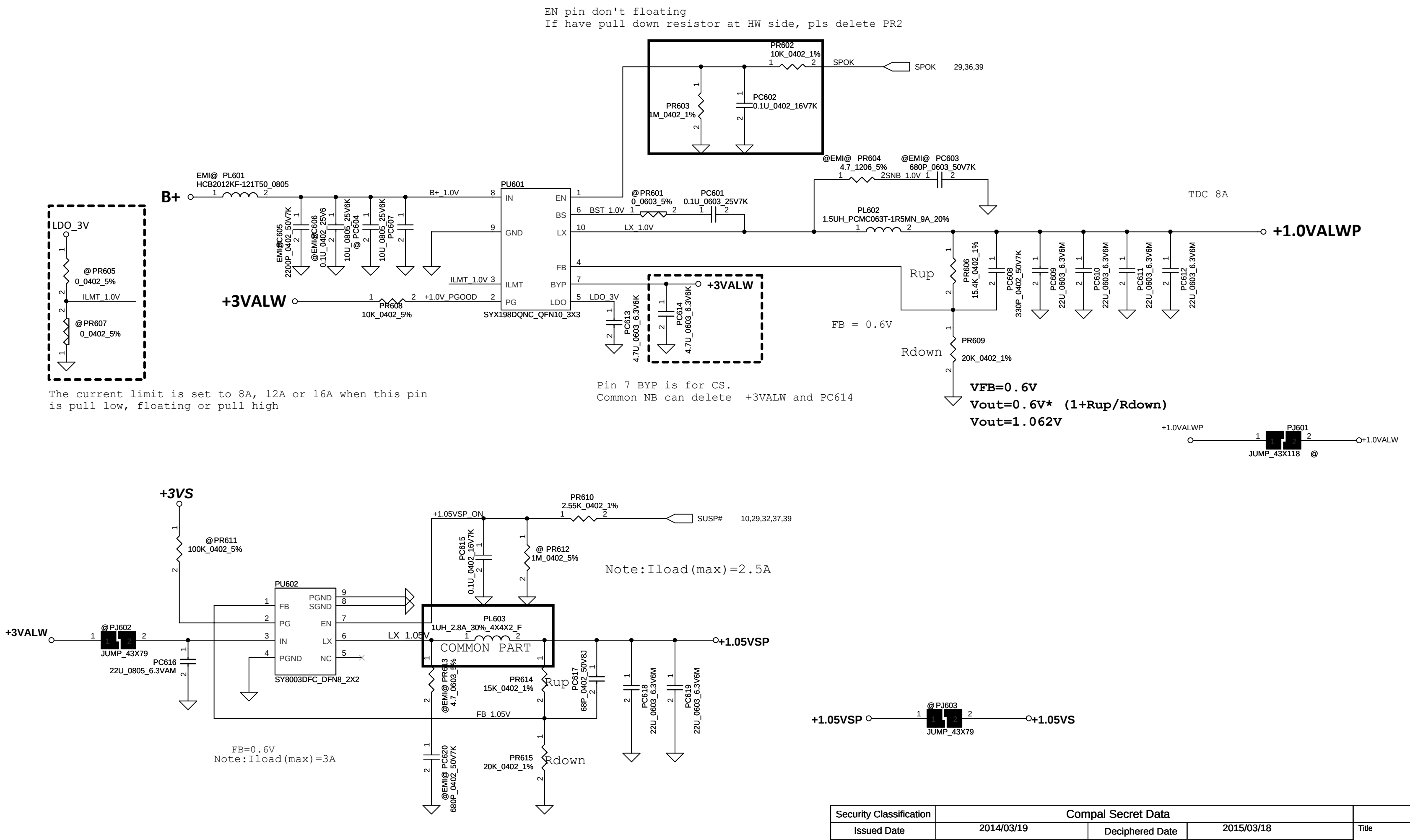
Note: S3 - sleep ; S5 - power off

Security Classification	Compal Secret Data		
Issued Date	2014/03/19	Deciphered Date	2015/03/18

Compal Electronics, Inc.

Title: 1.35VP/0.675VSP

Size: Custom | Document Number: A5WAM_Bay Trail M_LA-B981P | Rev 0.1



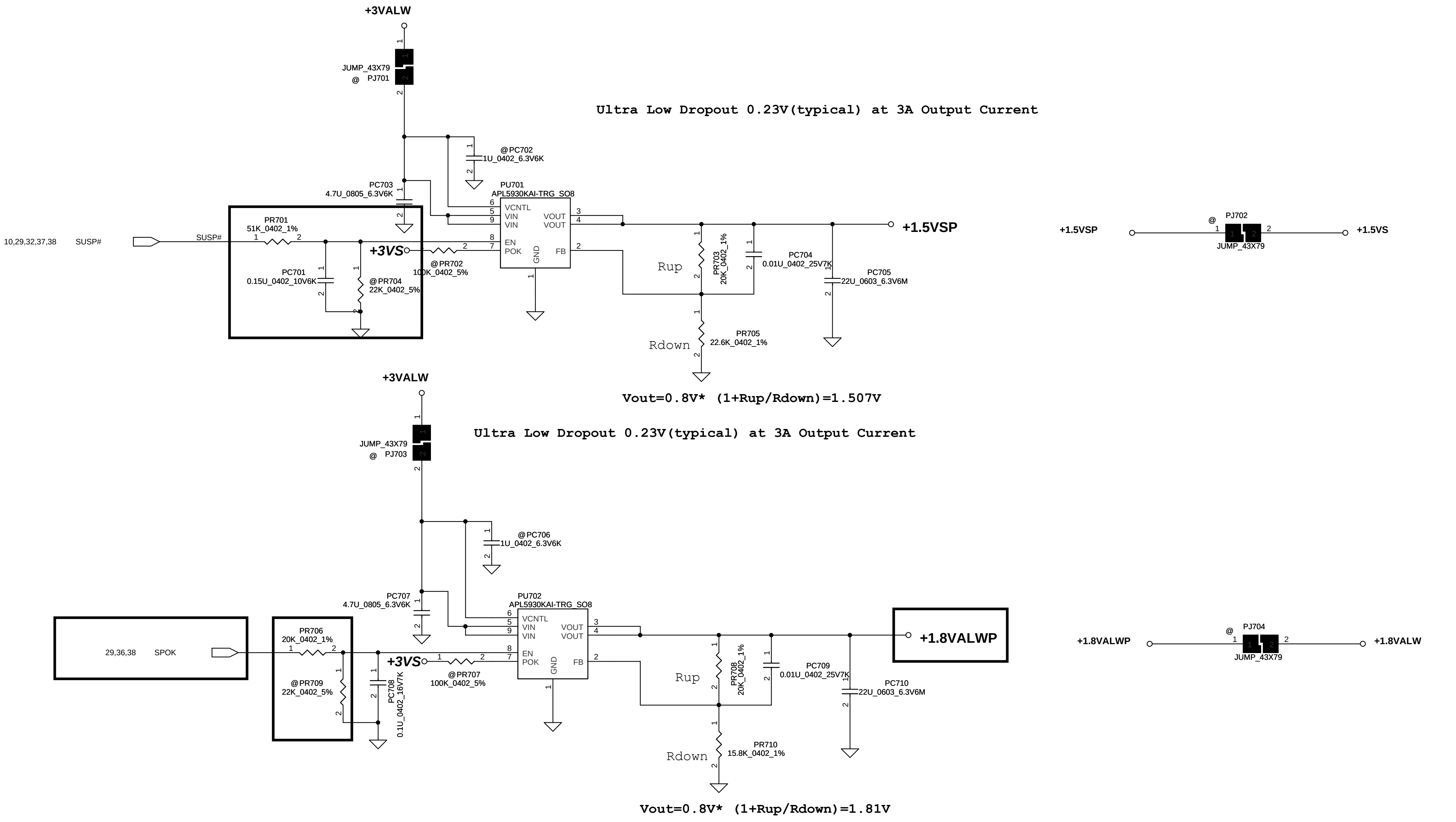
Security Classification	Compal Secret Data		
Issued Date	2014/03/19	Deciphered Date	2015/03/18

Compal Electronics, Inc.

Title: 1.05VS/1.0VALW

Size: C | Document Number: **A5WAM_Bay Trail M_LA-B981P** | Rev: 0.1

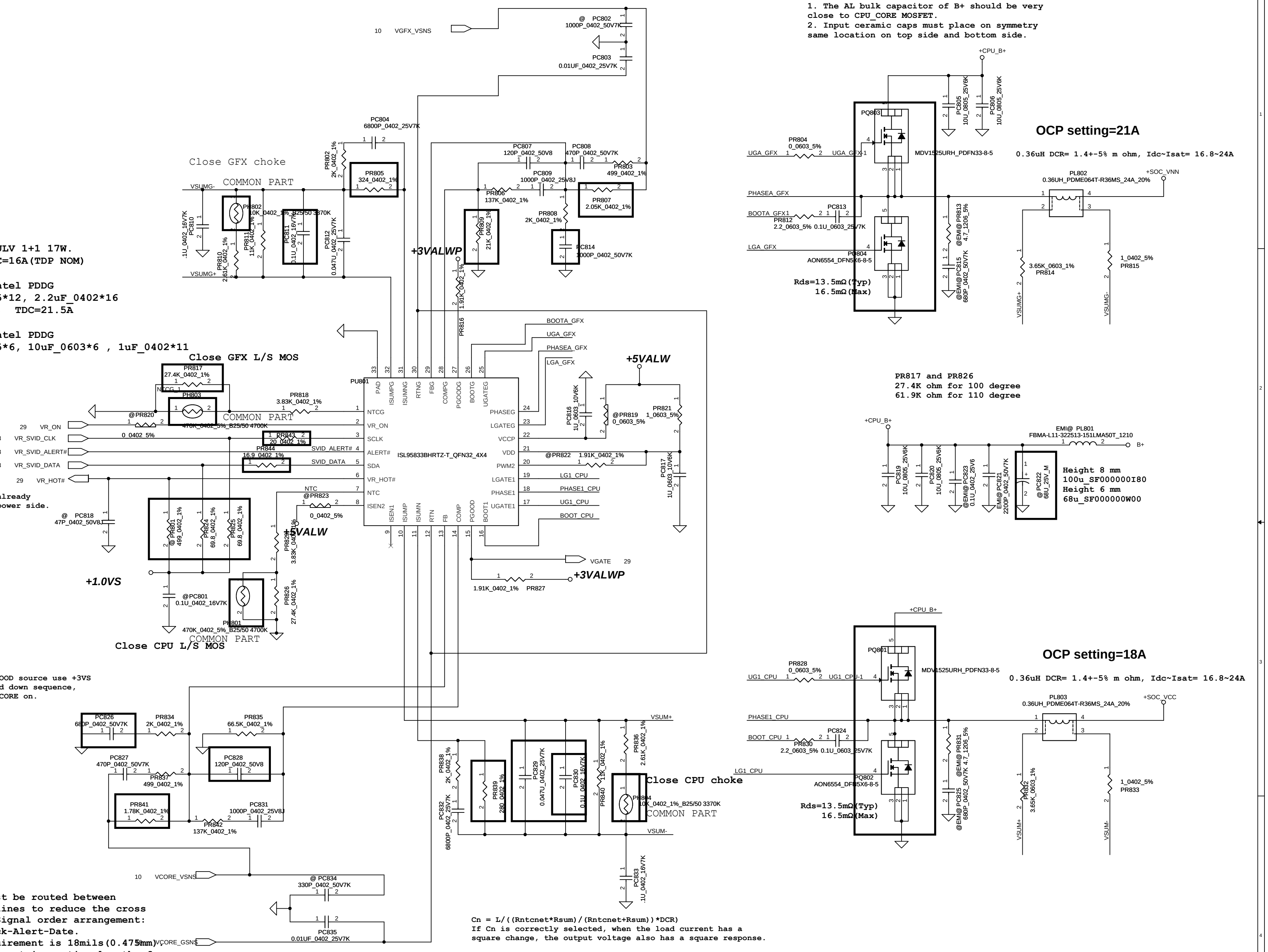
Date: Monday, May 12, 2014 | Sheet 38 of 47



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2014/03/19	Deciphered Date	2015/03/18	Title: 1.5VSP/1.8VALWP
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				Date: Monday, May 12, 2014; Sheet 39 of 47

Layout Note
Reduce Acoustic Noise
1. The AL bulk capacitor of B+ should be very close to CPU_CORE MOSFET.
2. Input ceramic caps must place on symmetry same location on top side and bottom side.

Design Note
This circuit is for ULV 1+1 17W.
CPU: IccMax=33A, TDC=16A(TDP NOM)
Loadline: -2.9 m V/A
Output Cap. follow Intel PDDG
330uF/9m*3, 22uF_0805*12, 2.2uF_0402*16
GFX(GT2): IccMax=33A, TDC=21.5A
Loadline: -3.9 m V/A
Output Cap. follow Intel PDDG
330uF/9m*2, 22uF_0805*6, 10uF_0603*6 , 1uF_0402*11



VDD source use +5VS and PGOOD source use +3VS
Please confirm power on and down sequence,
make sure VGATE after CPU_CORE on.

Cn = L/((Rntcnet*Rsum)/(Rntcnet+Rsum))*DCR)
If Cn is correctly selected, when the load current has a square change, the output voltage also has a square response.

Layout Note
SVID routing
1. Alert# signal must be routed between the Clock and Date lines to reduce the cross talk between them. Signal order arrangement: mobile order is Clock-Alert-Date.
2. SVID spacing requirement is 18mils(0.475mm).
3. Maximum total microstrip routing length of each SVID signal must not exceed 6000mils(152.4mm).
4. The SVID bus must be ground reference, It cannot be referenced to input (Vbat or 12V) power plans as they can couple noise into the SVID bus as power states change.
5. Avoid routing under noisy circuit, e.g. switch node , Gate driver, B+, Vin, high speed signal.
6. When SVID signal changes Layer, GND return path may be changed also. We need add GND via for GND reference.

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2014/03/19	Deciphered Date 2015/03/18	Title: CPU_CORE/GFX_CORE
			Size: Custom; Document Number: A5WAM_Bay Trail M_LA-B981P; Rev 0.1
			Date: Monday, May 12, 2014; Sheet 40 of 47

PWR Rule
需確認最新SPEC.
Modify 8/6.

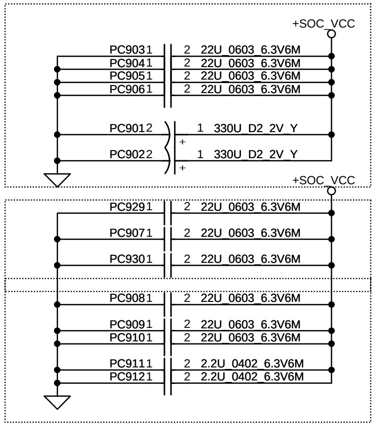
3 X 330u/9m(47W)
2 X 330u/9m(37W)
24 pcs 22uF and reserve 4 pcs
2013/08/16

+SOC_VCC =+CPU_CORE

Output Cap
(330uF*2+22uF*4)

Package Edge Cap
(22uF*3)

Back Side Cap
(10uF*1+4.7uF*2+2.2uF*2)

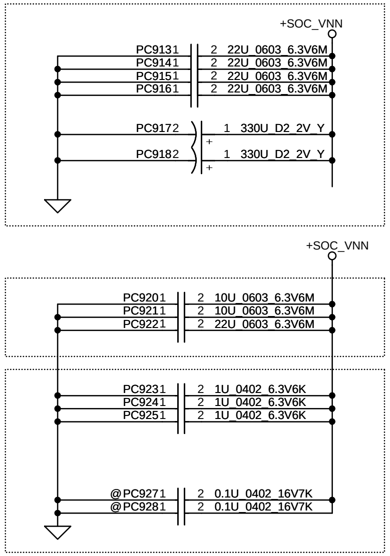


+SOC_VNN =+VGFX_CORE

Output Cap
(330uF*3+22uF*4)

Package Edge Cap
(22uF*3)

Back Side Cap
(1uF*3)



Security Classification	Compal Secret Data		
Issued Date	2014/03/19	Deciphered Date	2015/03/18

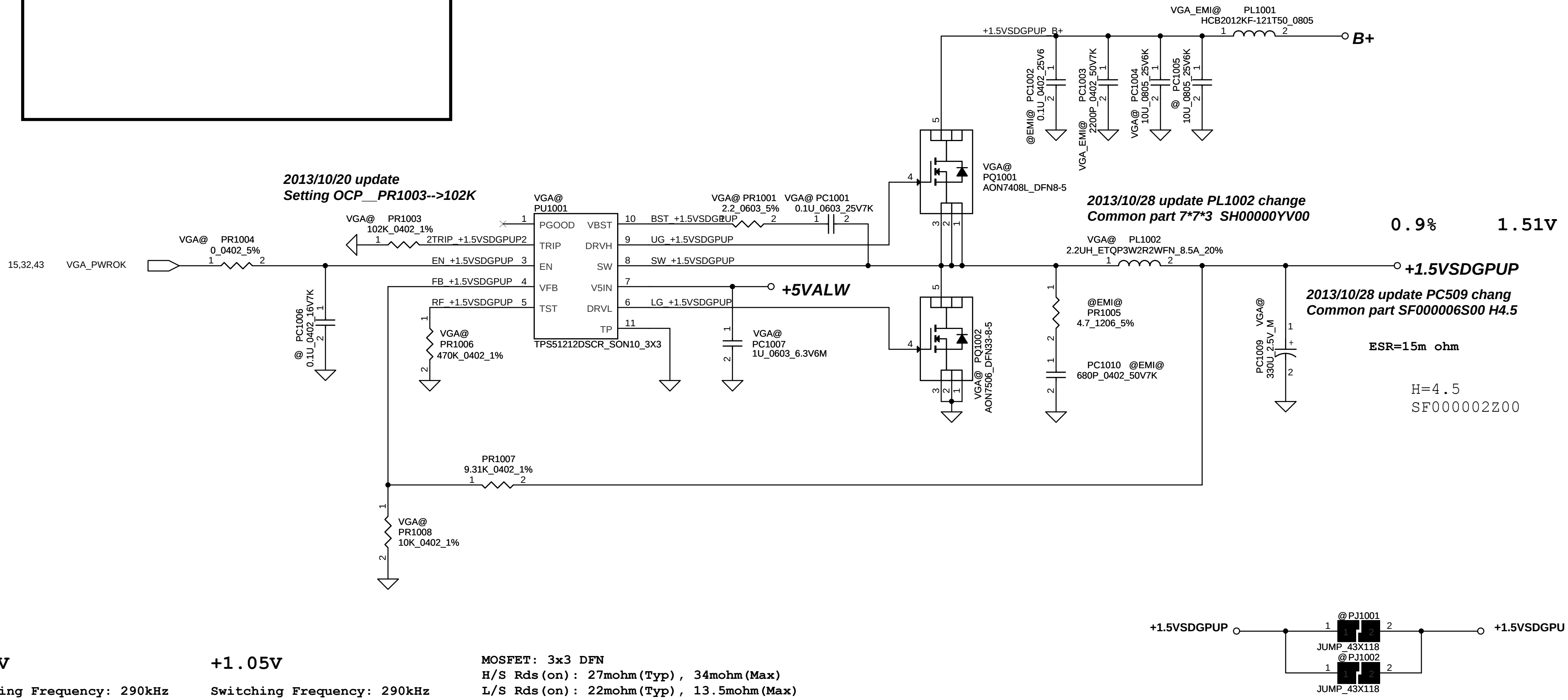
Compal Electronics, Inc.

Title: CPU/GFX capacitor

Size	Document Number	Rev
Custom	A5WAM_Bay Trail M_LA-B981P	0.1

Module model information

TPS51212_V1.mdd for Single layer
TPS51212_V2.mdd for Dual layer



+1.2V

Switching Frequency: 290kHz
Imax=8A
OCP~10.5A
OVP: 120%~130%
VFB=0.704V, Vout=1.207V

+1.05V

Switching Frequency: 290kHz
Imax=5.4A
Ipeak=6.5A
Iocp=7.8A
OVP: 120%-130%
VFB=0.704V, Vout=1.055V

MOSFET: 3x3 DFN
H/S Rds(on): 27mohm(Typ), 34mohm(Max)
L/S Rds(on): 22mohm(Typ), 13.5mohm(Max)

Choke: 7x7x3
Rdc=15.5mohm +/-15%

Switching Frequency: 290kHz
Ipeak=10A
Delta I =2.16A
Iocp=12.14~16.67A
OVP: 120%~130%
VFB=0.704V, Vout=1.51V

Vout	PR1007	PR1008	PR1003
+1.5V	11.5k	10k	
+1.35V	9.31k	10k	
+1.2V	7.15K	10k	105K
+1.05V	4.99k	10k	93.1k

Security Classification	Compal Secret Data		
Issued Date	2014/03/19	Deciphered Date	2015/03/18

Compal Electronics, Inc.

Title: 1.5VSDGPUP

Size: Custom | Document Number: A5WAM_Bay Trail M_LA-B981P | Rev: 0.1

Module model information:
RT8813A_V1A for IC module
RT8813A_V1B for SW module

Vboot=Vvref*Rref2/(Rref1+Rref2+Rboot)
Rt=Rrefadj // (Rboot+Rref2)
Vmin= Vvref*[Rref2/(Rref2+Rboot)]*[Rt/(Rref1+Rt)]
Vmax=Vvref*Rref2/[(Rref1//Rrefadj)+Rboot+Rref2]
Vout=Vmin+N*Vstep
Vstep=(Vmax-Vmin)/Nmax

PWM-VID Spec and component Values

PWM-VID Spec		Config B	Config C	Config D
Vmin		0.6V	0.65V	0.9V
Vmax		1.2V	1.15V	1.15V
Vboot		0.9V	0.9V	1.028V
Voltage step		6.25mV	25mV	12.5mV
N of Voltage level		96	20	20
Rrefadj	PR1206	20K	39K	27K
Rref1	PR1204	20K	30K	7.5K
Rboot	PR1205	2K	3K	0
Rref2=PR1209 +PR1212	PR1209	18K	24K	6.2K
	PR1212	0	3K	1.74K
C	PC1209	2.7nf	1.8nf	5.6nf
		N15S-GT	N15V-GL	N15V-GM

Current Limit threshold setting
Rocset= (Ivalley * Rds(on) + 40 mV) / 10uA

I_ripple=(19-0.9)*0.9/
(304.89Khz*0.36u*19)=7.811A

OCP=54A/2=27A per phase
Ivalley=27A-7.811A/2=23.1A

H-side MOS:AON6552
Rds(on):
5.6mohm@Vgs=10V
6.7mohm@Vgs=4.5V
Id :20A@Ta=25 degC

L-side MOS:AON6554
Rds(on):
3.2mohm@Vgs=10V
3~3.8mohm@Vgs=4.5V
Id :85A@Ta=25 degC

Choke: 0.22uH (Size:7*7*4)
Rdc=0.97mohm +-5%
Heat Rating Current=34A
Saturation Current=25A

C=3*330uF (9mohm)=990uF
Vripple=Iripple*ESR(min)=7.811A*3mohm=23.4mV

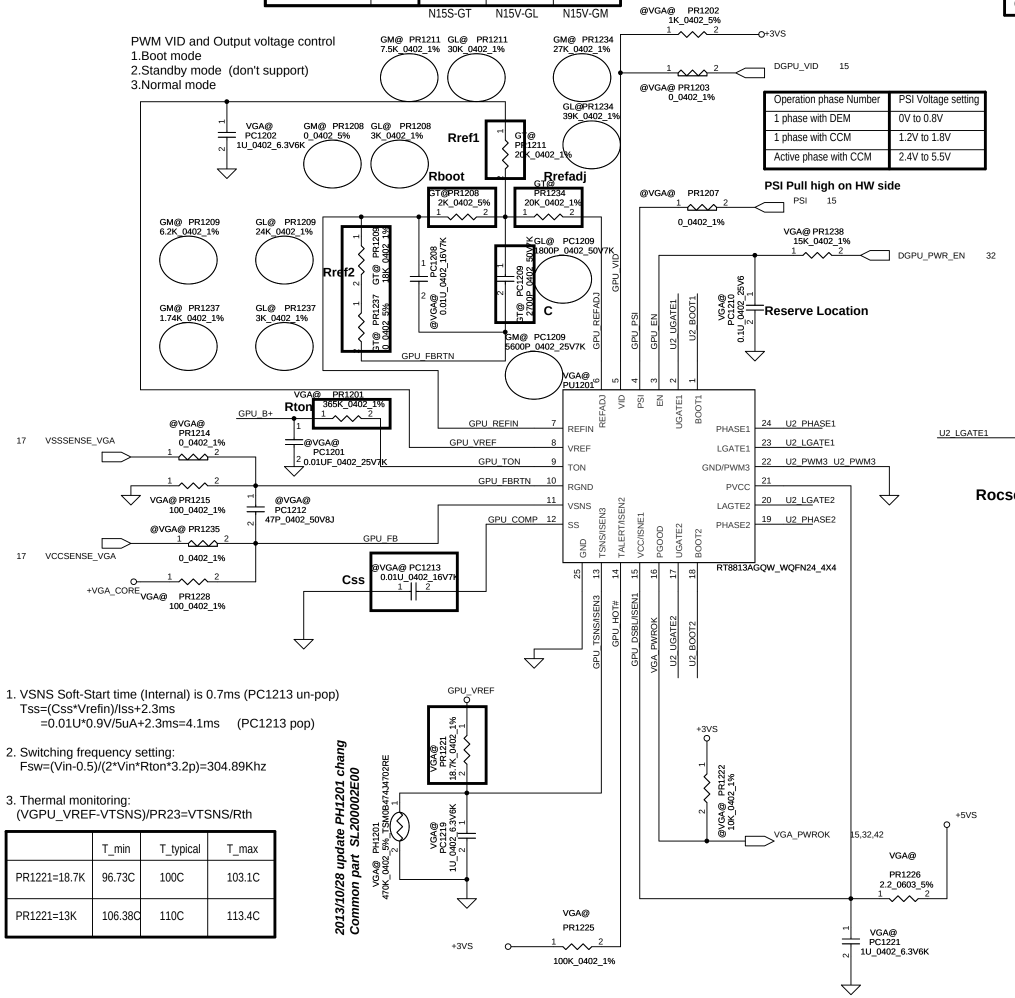
Different VGA Chip (different EDP-Peak Current) need select different solution

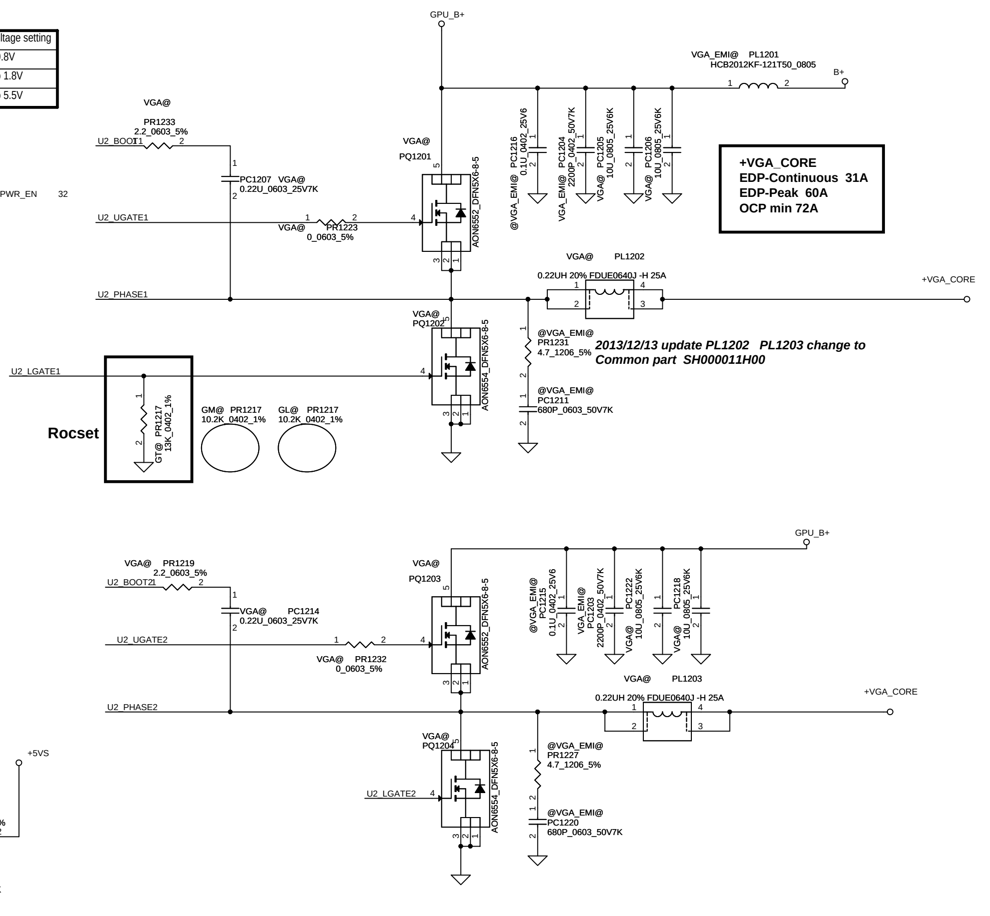
VGA Chip	N14P-GV	N14P-GV2	N14M-GS	N14M-LP	N14P-LP	N14P-GE	N14P-GS	N14P-GT	N15S-GT	N15V-GM
OpenVReg Configurations	Config B	Config B	Config B	Config B	Config B	Config B	Config B	Config B	Config B	Config C
Rated TDP Power at Tj=102C	18W	25W	18W	13W	18.9W	25W	25.6W	35.5W	18W	18.16W
Boosted GPU Total at Tj=102C	25W	32W	25W	20W	23W	N/A	30W	40W	25W	24.72W
EDP-Continuous at Tj=102C	24A	32A	26A	22A	25A	27A	38A	45A	31A	29.2A
EDP-Peak at Tj=102C	35A	55A	45A	35A	35A	40A	60A	75A	60A	44.3A
Istep max (Evaluation)	15A	27A	25A	20A	14A	12A	31.5A	35A		
OCP Setting Current	42A	66A	54A	42A	42A	48A	72A	90A	72A	54A
Rocset	8.96K	12.45K	10.7K	8.96K	8.96K	9.83K	8.3K	9.39K	13K	10.2K
Recommendation	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H2L	2phase 1H2L	2phase 1H1L	2phase 1H1L
Polymer Cap (330uF)	6mohm * 2	9mohm * 3	9mohm * 3	6mohm * 2	6mohm * 2	6mohm * 2	6mohm * 3 (L=0.22uH)	4.5mohm * 3 (L=0.15uH)		
Or OSCON (390uF)	10mohm * 3	10mohm * 3	10mohm * 3	10mohm * 3	10mohm * 3	10mohm * 3	NULL	NULL	GT@	GM@

PWM VID and Output voltage control
1.Boot mode
2.Standby mode (don't support)
3.Normal mode

Operation phase Number	PSI Voltage setting
1 phase with DEM	0V to 0.8V
1 phase with CCM	1.2V to 1.8V
Active phase with CCM	2.4V to 5.5V

PSI Pull high on HW side





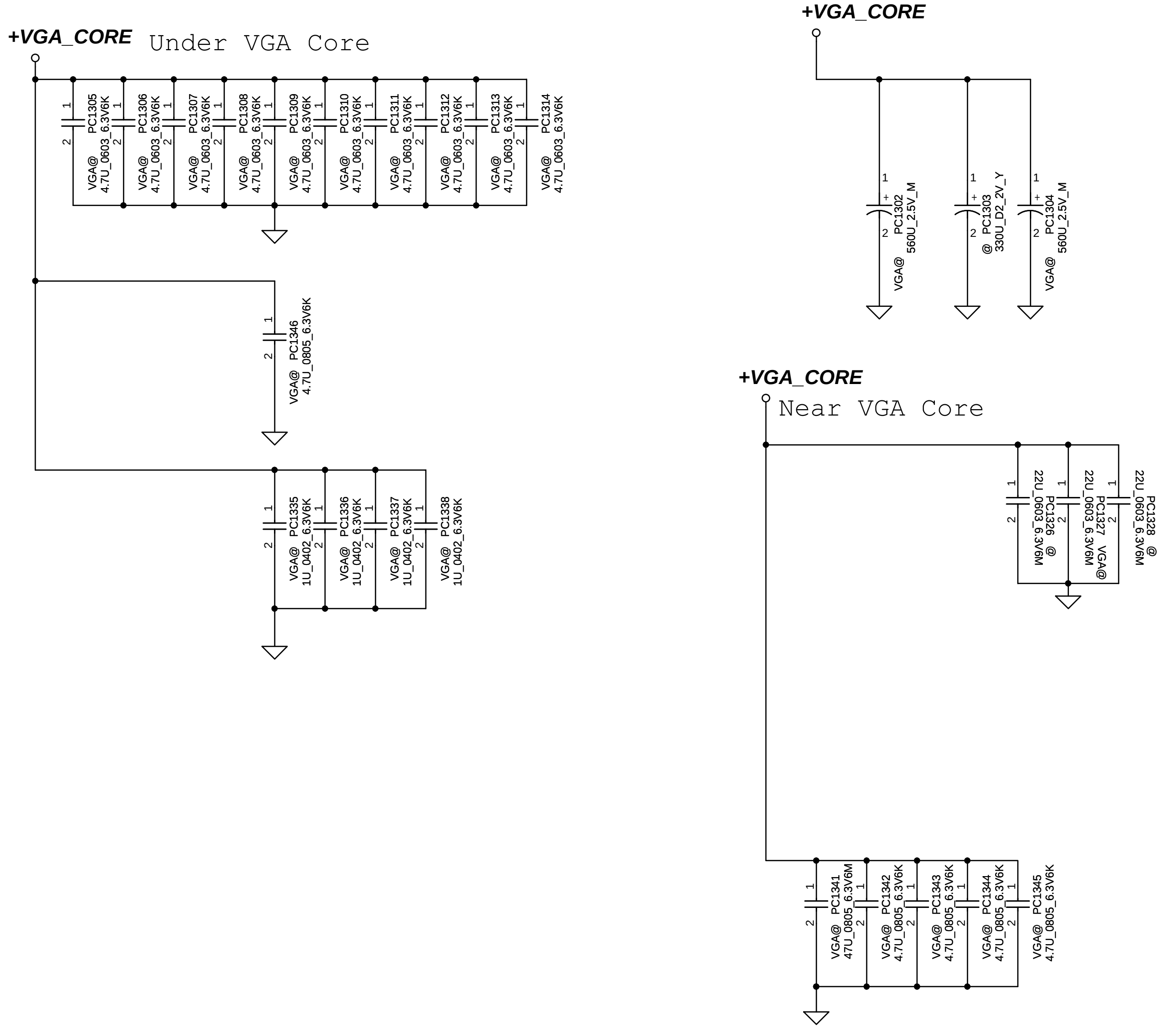
+VGA_CORE
EDP-Continuous 31A
EDP-Peak 60A
OCP min 72A

1. VSNS Soft-Start time (Internal) is 0.7ms (PC1213 un-pop)
   Tss=(Css*Vrefin)/Iss+2.3ms
   =0.01U*0.9V/5uA+2.3ms=4.1ms (PC1213 pop)

2. Switching frequency setting:
   Fsw=(Vin-0.5)/(2*Vin*Rton*3.2p)=304.89Khz

3. Thermal monitoring:
   (VGPU_VREF-VTSNS)/PR23=VTSNS/Rth

	T_min	T_typical	T_max
PR1221=18.7K	96.73C	100C	103.1C
PR1221=13K	106.38C	110C	113.4C



N15x 2013/12/10
Under
4.7uF_0603_10pcs
1uF_0402_4pcs
Near
47uF_0805_1pcs
22uF_0603_1pcs(2PCS unpop)
4.7uF_0805_5pcs

N15x2013/10/17
Under
4.7uF_0603_15pcs
1uF_0402_8pcs
Near
47uF_0805_0pcs
22uF_0603_9pcs(2PCS unpop)
4.7uF_0805_5pcs

N15x2013/10/07
Under
4.7uF_0603_15pcs
1uF_0402_8pcs
Near
47uF_0805_0pcs
22uF_0805_9pcs(2PCS unpop)
4.7uF_0805_5pcs

N15x2013/10/02
Under
4.7uF_0603_15pcs
1uF_0402_8pcs
Near
47uF_0805_0pcs
22uF_0805_14pcs
4.7uF_0805_5pcs

N14x
Under
4.7uF_0603_10pcs
0.1uF_0402_4pcs
Near
47uF_0805_1pcs
22uF_0805_1pcs
4.7uF_0805_5pcs

Security Classification	Compal Secret Data		
Issued Date	2014/03/19	Deciphered Date	2015/03/18

Compal Electronics, Inc.

Title: VGA_CORE CAP

Size: Custom | Document Number: A5WAM_Bay Trail M_LA-B981P | Rev: 0.1

Date: Monday, May 12, 2014 |

Version change list (P.I.R. List)

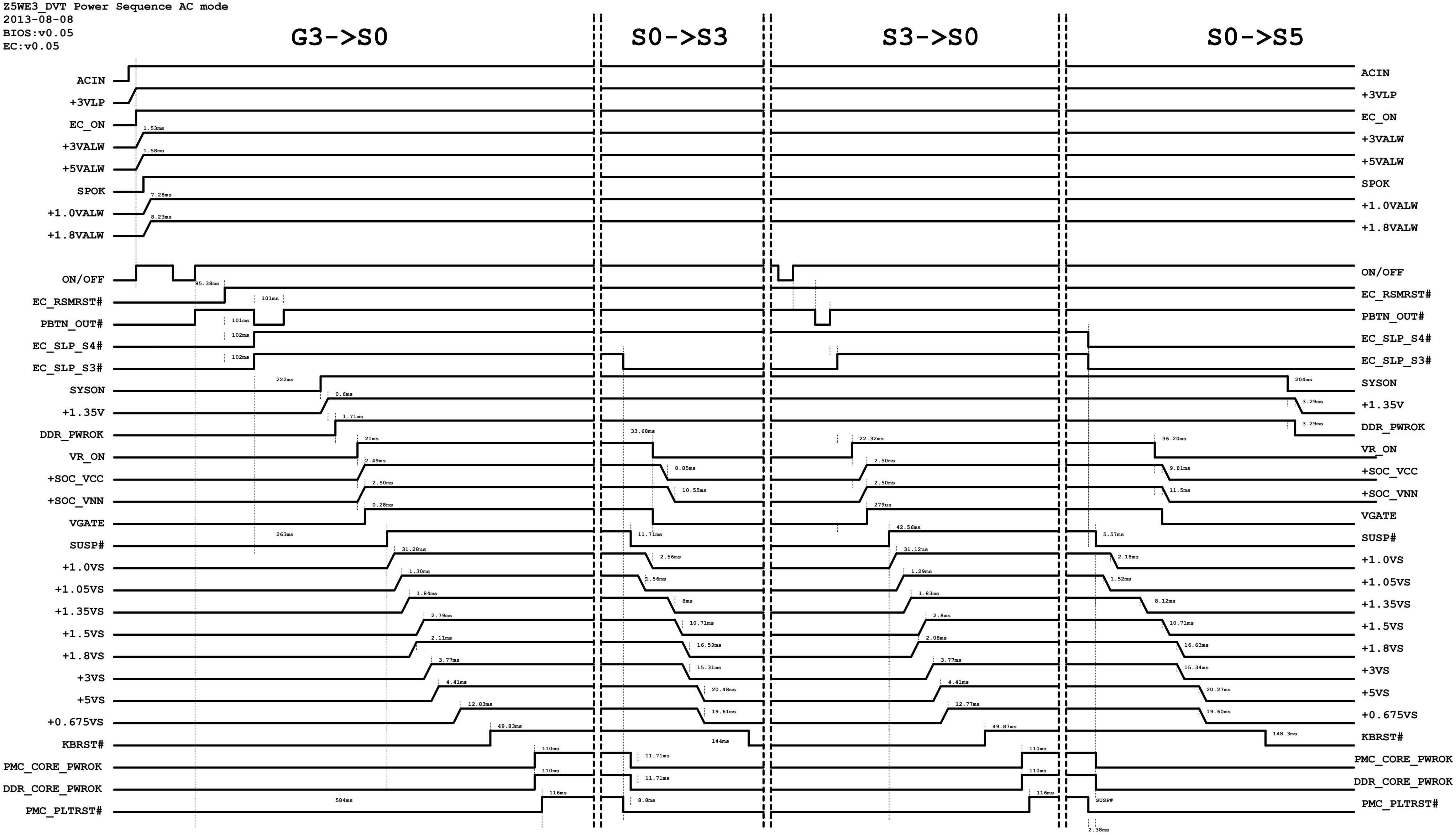
Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	CPU tranistion			40	PR839 change to 280 ohm	4/9	DVT
2	NV power sequence			43	PR1222 VGA@->@VGA@	4/9	DVT
3					PR1238 0->15K_0402_1%	4/9	DVT
4							
5					PC1210 pop 0.1U(SE00000G880)	4/9	DVT
6	For EMI test			42	PR1007 change to 9.31K	4/23	PVT
7	unused part			38	PR607 change to R-Short 0402	4/23	PVT
8					PR601 change to R-Short 0603	4/23	PVT
9				36	PR407 change to R-Short 0603	4/23	PVT
10	For voltage adjust			38	PR606 change to 15.4K	5/6	PVT
11							
12							
13							
14							
15							
16							
17							
18							

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2014/03/19	Deciphered Date	2015/03/18	Title: PWR_PIR
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Version Change List (P. I. R. List) Page 1/1 for HW

Item	Page#	Function	Date	Request Owner	Issue Description	Solution Description	Rev.
1	P.6/8/28/32	HW	5/8		Fix S3/S5 have pluse at singal	U63.5/U58.5/U53.5/U62.5/U64.5 change power source from +1.8VS to +1.8VALW	0.2
2	P.8/15/29	HW	5/8		Change R-short for cost down	R236,R237 change to R-Short 0805 R1044 change to R-Short 0402 R1015 change to R-Short 0402	
3	P.31	HW	5/8	EMI	Request from EMI add Bead at speaker	R1094/R1095/R1096/R1097 change from 0ohm to BEAD(SM01000CC00)	
4	P.29	HW	5/8		Change EC version to latest	change EC U28 to SA000075S30(KB9022QD) R506 change from 130K->160K_0402_1%(SD034160380)	
5	P.9	HW	5/8		Add for Debug	ADD R973 0_0402_5%(@) at USB_HUB reset (connect to SYSON) ADD R1176/R1173 0_0402_5% for DGPU_PWR_EN_SOC1.8V ADD R1175/R1174 0_0402_5% for DGPU_HOLD_RST#_SOC1.8V ADD JP2@ R1081@ R1082@(for debug)	
6	P.15	HW	5/8		Add PH resistor	R1043 change from 0ohm->10K_0402_5% unpop R2018(DGPU_HOLD_RST#_SOC1.8V) PH resistor	
7	P.11	HW	5/8		change cap to improve +1.0VS power rail	C1056 C1057 C1059 change footprint from 22U_0805->0603	
8	P.4	HW	5/8		Update DA P/N	DA P/N change to DA60019D000	

Z5WE3_DVT Power Sequence AC mode
2013-08-08
BIOS:v0.05
EC:v0.05



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Title: Power Sequence		
Size: C	Document Number: A5WAM_Bay Trail M_LA-B981P	Rev: 0.1
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